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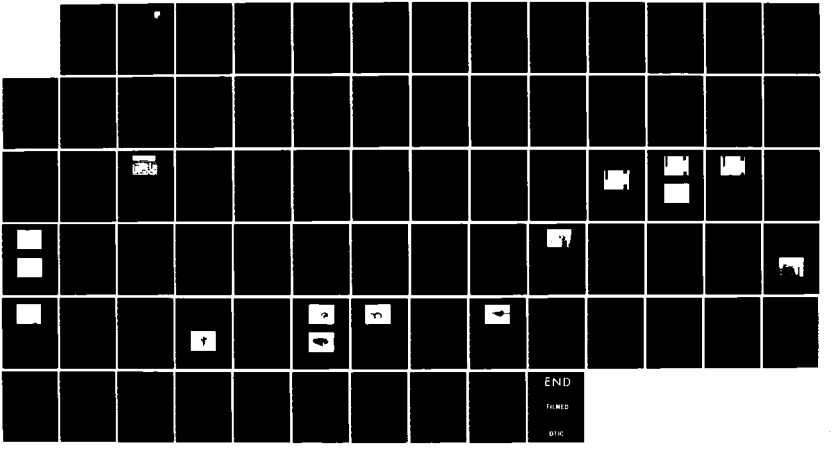

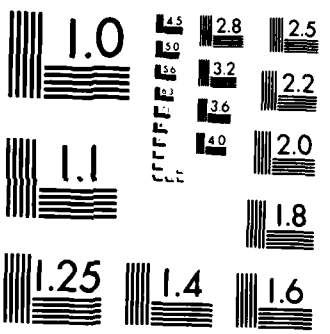

RADC-TR-85-17
Final Technical Report
February 1985

SILICIDE CONDUCTORS RELIABILITY RESEARCH

RCA Laboratories

T. J. Faith

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An investigation into the reliability of polycide conductors has been performed utilizing highspeed CMOS logic circuits (QMOS) and a parametric test circuit, the contact-resistance test vehicle (CRTV). The hermetically-packages QMOS units were split into control- and test-circuit groups; control circuits utilizing standard QMOS processing with n^+ polysilicon gates, test circuits utilizing n^+ polysilicon/$TaSi_2$ (polycide) gates. Relevant features of the CRTV include long, narrow (2.5 μm to 3 μm) polycide lines connected to overlying Al or Al-1%Si Kelvin-contact patterns through small (1.5 μm x 1.5 μm to 2 μm x 2 μm) interlevel contacts, and large (600 μm x 600 μm) polycide/oxide/silicon capacitors, the (3000 Å polysilicon/1600 Å $TaSi_2$) polycide being separated from the silicon substrate by an unpatterned, 500 Å steam-grown gate oxide.

No significant degradation in either CRTV polycide line integrity or CRTV gate-oxide breakdown strength was experienced during 30 cycles of thermal shock (-70°C to +100°C). (over)

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No failures or significant parametric degradations were experienced by a group of 100 QMOS circuits (50 test/50 control) subjected to 1000 temperature cycles (-65°C to +150°C). Four failures (1 test/3 control) were experienced by a group of 54 QMOS circuits (27 test/27 control) during static-bias, step-stress testing for 168 hours at 125°C, 150°C, 175°C, 200°C and 250°C. The single test-unit failure, which occurred dur to increased leakage current after the 250°C test increment, was traced to an in-process scratch in the gate oxide. None of the 50 surviving units experienced significant parametric degradation.

Results of high-current CRTV testing have identified the weak link in the polycide/Al-alloy bilevel structure to be the $TaSi_2$/Al-alloy contact interface. Units with good contacts ($<1.5 \times 10^7$ A/cm^2, which result in (joule-heated) mean polycide-line temperatures of $\gtrsim$ 400°C. No significant pre-failure degradation in line resistance was observed in these failures, and pre-failure contact-resistance degradation was always less than 5 ohms.

In contrast, failure levels decrease rapidly with increasing initial contact resistance for units with values above approximately 1 ohm, failures occurring at values as low as 5×10^6A/cm^2 and 90°C. Such early failures are highly localized at contacts, whereas in the $\gtrsim$ 400°C failures, visible line damage extends outward for distances up to several hundred micrometers from the contacts with evidence of substantial Al migration along visibly damaged polycide line segments, of Ta loss along damaged line segments, and of Ta buildup at ontact sites. Both types of failure show evidence of intense local heating at contacts, with Al melting (660°C) being occasionally visible. Polarity effects are empirically consistent but complex, early failures occurring at the negatively biased contact; $\gtrsim$ 400°C failures, at the positibely biased contact.

The finding that the relatively modest $TaSi_2$/Al-alloy initial contact resistance of $\gtrsim$ 1 ohm represents a significant threat to circuit reliability makes it imperative to perform individual contact-resistance measurements at wafer-acceptance test (WAT) for circuit types which pass substantial interlevel currents.

FINAL REPORT EVALUATION

SILICIDE CONDUCTORS RELIABILITY RESEARCH

This effort investigated the failure mechanisms associated with $TaSi_2$ polycide conductors. The testing was performed on an SSI CMOS circuit and on a contact resistance test vehicle. CMOS circuits with polysilicon gates were used as controls for the SSI CMOS circuits. No failure mechanisms were revealed by comparing the test results of the polysilicon and tantalum silicide CMOS circuits. The contact resistance test vehicles revealed failure mechanisms associated with aluminum alloy-tantalum silicide contacts.

The author points out the necessity for careful evaluation of contact resistances as a screen for early contact failures. Further work indicated by this effort includes testing to sort temperature and current effects, more intense studies of ionic motion in tantalum silicide conductors to sort electric field and current forces, and investigations of discrepancies between 1mA measurement and in-situ measurement of the resistance change in contact strings.

This effort indicates the critical nature of contact stability in VLSI microelectronic reliability, and points to a need for a more basic understanding of contacts and their degradation

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Reliability Physics Section
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I. INTRODUCTION

The requirements in very-large-scale integrated circuitry (VLSI) for a ate-level material with low resistivity and a high-temperature processing apability has been thoroughly discussed in the literature [1-4]. The effort o achieve this goal has centered on replacement of the customary n^+-poly- ilicon gate material by an n^+-polysilicon/refractory-metal-silicide composite polycide). The principal candidate materials are four refractory-metal lisilicides, i.e., $MoSi_2$, $TaSi_2$, $TiSi_2$, and WSi_2.

There is a growing body of reports on polycide processing steps such as leposition [5-9], silicide anneal [3,8-10], oxidation[11-14], and pattern lefinition [15-17]; and on process-related properties such as resistivity [2-4,18], film structure [18], and stress [3,19-21]. Process-associated effects which have been reported include dopant diffusion from polysilicon into the silicide during silicide anneal and oxidation [22,23], and polysilicon undercutting during the pattern etching of the polycide composite [15,17]. Influences of processing conditions on silicide integrity [24] and dielectric integrity [11,14,25] have also been reported.

These process-oriented investigations, many of which uncovered reliability implications, have been accompanied by direct reliability studies, some of wh[illegible] involved accelerated testing of special test structures [26,27], while [illegible]s ncerned comparisons between standard polysilicon-gate MOS circuits and similar units with polycide gates [28-30].

This body of literature, together with the polycide process-development efforts at RCA [9,10,22], furnished background information for the present program which is aimed at determining the predominant failure mechanisms associated with polycide gate conductors, evaluating their impact on VLSI reliability, and recommending process and test procedures to mitigate their impact.

RCA had chosen to develop a polycide gate process for MOS circuitry based on $TaSi_2$, which has the advantages of a lower resistivity than either $MoSi_2$ or WSi_2 and a better compatibility with hydrofluoric-acid processing than $TiSi_2$. Consequently, n^+ polysilicon/$TaSi_2$ was the logical choice for the present program, providing an in-house processing capability and a data base on in-process film characteristics.

(or improvement) in delay time for both test and control groups during cycling in three of the four delay times.

TABLE I

N-channel and P-channel threshold distributions, QMOS polycide test units and polysilicon control units: Pre- and post-1000 temperature cycles.

	N-CHANNEL TRANSISTORS		
THRESHOLD VOLTAGE (V)	0.76	0.80	0.84
TEST (INITIAL)	9	25	16
TEST (1000 CYCLES)	9	26	15
CONTROL (INITIAL)	4	41	5
CONTROL (1000 CYCLES)	4	43	3

	P-CHANNEL TRANSISTORS					
THRESHOLD VOLTAGE (V)	1.08	1.12	1.16	1.20	1.24	1.28
TEST (INITIAL)	1	8	25	16		
TEST (1000 CYCLES)	2	11	27	10		
CONTROL (INITIAL)			2	20	26	2
CONTROL (1000 CYCLES)			2	20	28	

2. Step-Stress Testing.

A total of three polysilicon-gate control-group units and one polycide-gate test-group unit experienced failure during the bias-life, step-stress tests. Two of the control units failed at 200°C; the third failed at 225°C. All three control units failed in several test modes, including leakage and [illegible] tional test. The lone test-unit failure appeared in the input-breakdown test after the 250°C stressing increment. It was a parametric (high leakage) failure, not a catastrophic failure, permitting final measurement of threshold voltages and propagation delays. These parameters are listed for test and control units in Tables III and IV, respectively, which follow the same formats as Tables I and II. The results are similar to those in Tables I and II, the threshold showing excellent stability, and the delay times showing slight

IV. RESULTS AND DISCUSSION

A. QMOS CIRCUIT

One-hundred packaged polycide-gate test units and an equal number of polysilicon-gate control units were submitted for reliability tests. All of these units were subjected to the first level of step-stress bias-life testing, i.e., 168 hours at 125°C. The purpose was to determine if there were any early failures. When post-125°C electrical tests showed that there were no failures, the first 50 units of each group were submitted for temperature cycling; the next 27 of each group, for 150°C to 250°C step-stress tests.

1. Temperature Cycling.

No failures occurred in either the test group or the control group during the 1000 temperature cycles. Table I shows a statistical listing of the n-channel and p-channel transistor thresholds for each group measured initially and after 1000 cycles. Each column in this table represents a 0.04 V increment in threshold voltage, ranging from 1.08 V to 1.32 V for the p-channel transistors and from 0.76 V to 0.84 V for the n-channel transistors. The number under each increment represents the number of units whose threshold falls within that increment. The initial n-channel threshold distribution for both groups is centered at 0.80 V, remaining there throughout cycling.

The p-channel threshold distribution for the polycide-gate test group is centered at 1.16 V, approximately 0.06 V below that for the polysilicon-gate control group, and both groups showed excellent stability during cycling.

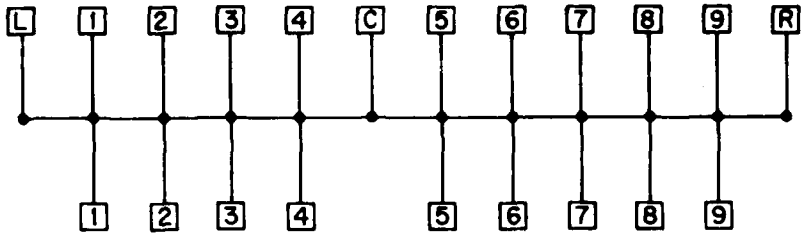
Four different propagation delays were measured for each unit at each check point in the experiment. Table II lists the initial and post-1000 cycle means and standard deviations for test and control groups for each of the delays measured (labelled 1 to 4 at the top row of the table). All values have units of nanoseconds, the maximum acceptable delay being 30 ns for all channels. The delay times are substantially lower for the polycide-gate test units than for the polysilicon-gate control units, both before and after the 1000 temperature cycles. However, the standard deviations are comparable for all groups, ranging from a low of 1.38 ns to a high of 1.84 ns. One interesting feature (for which we don't have an explanation at present) is a significant reduction

Current to the polycide lines (and $TaSi_2$/Al contact strings) was supplied by a Keithley model 225 Constant-Current Source. Voltage measurements were performed using a Hewlett-Packard model 3467A four-channel Logging Multimeter and a Keithley model 614 Electrometer.

The principal high-current testing procedure started with initial measurements at the standard (low) current value of 1mA. Power was then applied at progressively increasing current levels, maintaining each current level at a constant value for 10 minutes while taking in-situ measurements at the start of each powering increment and at 1-minute intervals thereafter. After each 10-minute powering increment, the current was reduced back to 1mA for monitoring readings. All initial, in-situ, and monitor measurements were those listed for the appropriate test mode in Fig. 5. Tests were typically performed at 10mA increments up to 50mA, and at 5mA increments above 50mA until a catastrophic failure was experienced.

Test modes 1 and 3 were used as monitors only, and were not used in the high-current testing. Mode-2 high-current tests were performed at room-temperature ambient and at 100°C and 200°C ambients. The high-current tests in modes 4 to 7 were all performed at room-temperature ambient. Failure sites on all participating chips were identified and photomicrographs were taken at 1000X magnification. Selected chips were prepared and submitted for scanning-electron microscopy (SEM), electron-probe microanalysis (EPM), and Auger-electron spectroscopy (AES).

Having established short-term failure levels in the 10-minute-increment testing, a number of chips were submitted to high-current testing at a constant current for periods of either 16 hours or 64 hours. The current levels for these tests were selected to be approximately 80 percent of the short-term failure levels. The objective of these tests, in addition to defining longer-term failure levels, was to provide samples for SEM, EPM, and AES which had been heavily powered, but had not experienced failure.



TEST MODE	CURRENT PATH	LINE RESISTANCE(S)	CONTACT RESISTANCE(S)
1	L-R	1-2 AND 3-4	NONE
2	L-3	1-2	3
3	C-8	6-7	8
4	1-4	2-3	1,4
5	3-4	3-4	3,4
6	1-2	1-2	1,2
7	C-4	C-4	4

Figure 5. Schematic diagram of CRTV polycide line, contacts and bond pads, with tabulations of electrical connections used in test modes 1 to 7.

polycide line segment 1-2 and exits at contact 2, with no intermediate contacts. The sign convention identifies the current-flow direction in these test modes as plus (+) for current flowing from left to right and minus (-) for current flowing from right to left. For example, in mode 5(+), contact 3 is the positive terminal, contact 4, the negative terminal.

Columns 3 and 4 of Fig. 5 list the line resistances and contact resistances, respectively, which are measured in-situ in each mode. In modes 1 to 4 the line resistances are measured across internal (non-current-carrying) voltage taps. These measurements are consequently "four-probe" measurements which are free from voltage contributions due to contact resistances.

However, in modes 5 to 7 these measurements were actually terminal-voltage measurements, including contact-resistance contributions from each contact. These contact resistances were measured and subtracted from the terminal voltage to arrive at the line resistance.

The measurement technique used to determine contact resistances has been presented elsewhere [36,38]. Briefly, it is a four-probe method in which the voltage drop measured directly across the contact interface is divided by the current drawn through the contact. For example, in mode 6 illustrated in Fig. 5, the contact resistance at contact 1 is measured by dividing the voltage between pad L and (upper) pad 1 by the current drawn between (lower) pad 1 and pad 2.

speed. Chips which had undergone thermal shock tests were also subjected to high current testing.

High-current testing on both unshocked and shocked chips was performed principally on contact-terminated segments of the polycide line (Fig. 3), with a limited number of additional tests being performed on the $TaSi_2$/Al contact strings (Fig. 4). Testing was performed on unpackaged chips with electrical contact being made through a probe card matched to the CRTV bond-pad layout.

Most of the testing was done at room-temperature ambient with the chip mounted on a unheated chuck, and with polycide-line temperature increases occuring through direct Joule heating. A smaller number of tests were run with a hot chuck, including a series of low-current measurements at several chuck temperatures from which the polycide temperature coefficient of resistance (TCR) was calculated [37]. The average TCR (25°C to 300°C) for the polycide film is approximately 2.7×10^{-4} $(°C)^{-1}$, a value consistent with TCRs reported elsewhere [4]. The line resistance value measured at room temperature likewise reflected a $TaSi_2$ resistivity consistent with literature values, i.e., 4.4×10^{-5} ohm-cm. The TCR measurement, together with in-situ line-resistance measurements, provided the basis for calculations of average line temperature during high-current testing.

In the $TaSi_2$/Al contact strings (Fig. 4), the only electrical connections are to the end terminals; consequently, the powering and measuring options are limited to this single electrical configuration. In contrast, the multiple electrical connections to the polycide line (Fig. 3) provide many options.

Figure 5 shows a schematic representation of the polycide line running horizontally and the Al interconnect lines running vertically, crossing at $TaSi_2$/Al contacts, and terminating in bond pads shown as squares at top and bottom. The numbers (letters) with which these bond pads are labelled in Fig. 5 represent the corresponding contacts, as labelled in Fig. 3.

Below the diagram in Fig. 5 are listed the seven different powering/measuring configurations used in the polycide-line high-current testing. The first column identifies the test mode number designation (modes 1 to 7). The second column specifies the current path through the polycide line by identifying the bond pads which serve as current taps. For example, in mode 1 current passes through the entire length of the polycide channel, entering at contact L, exiting at contact R, and passing by all contact interfaces from contacts 1 through 9, whereas in mode 6, the current enters at contact 1, passes through

III. ACCELERATED-TESTING PROCEDURES

A. QMOS CIRCUIT

The QMOS accelerated testing program was performed at the RCA Solid State Division (SSD), Somerville. The two tests selected for the QMOS portion of the polycide reliability program were (1) temperature cycling and (2) step-stress, bias-life testing. Fifty test and 50 control units were alloted for temperature cycling; 27 test and 27 control units, for step-stress testing. Temperature cycling was performed between -65°C and +150°C, for 25 minutes at each extreme, with 5-minute transfer times (air to air chambers). A total of 1000 cycles were performed, with electrical readings taken initially, and after 25, 50, 100, 200, 400, 600, 800, and 1000 cycles. Bias life tests (with supply voltage fixed at 6V) were performed for 168 hours at each of the following temperatures: 125°C, 150°C, 175°C, 200°C, 225°C, and 250°C, with electrical readings performed initially and after each temperature increment.

The initial and periodic electrical readings were performed at room temperature, covering a comprehensive set of parametric and functional tests including contact, input leakage, output current, output voltage, input breakdown, propagation delay, and n-channel and p-channel thresholds. Complete datalogs of all these measurements were printed. Failure analysis was performed on test units which experienced failure during these tests.

B. CRTV CIRCUIT

The two types of accelerated tests selected for the CRTV portion of this program were (1) thermal shock and (2) high-current, high-temperature powering of the polycide lines and contact strings. In the thermal shock tests, unpackaged chips were transferred between a boiling-water bath (+100 C) and a dry-ice/alcohol bath (-70 ± 3°C) for a total of 30 cycles. Hot-to-cold transfer time was less than 10 seconds; cold-to-hot transfer time, less than 15 seconds. Dwell time at each temperature was 5 minutes.

Measurements of polycide line resistance were performed initially and after 1, 5, 13 and 30 cycles on shocked units. Measurements of gate-oxide breakdown voltage were then performed on each of the six polycide capacitors on shocked chips. These were compared with corresponding measurements on unshocked chips. Catastrophic breakdowns were measured using a 10V/sec ramp

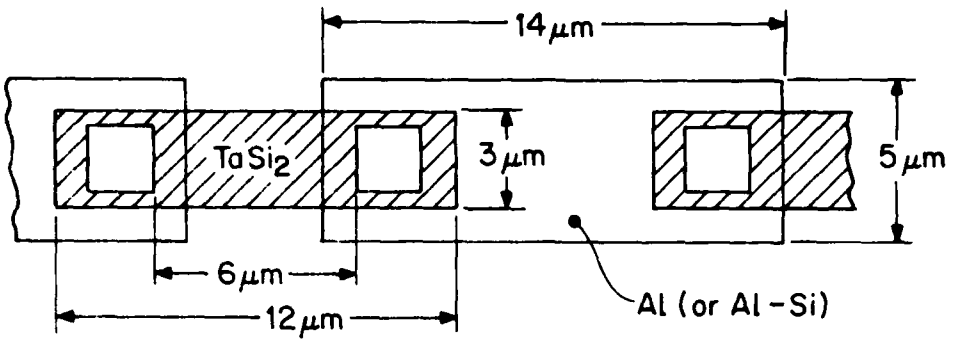


Figure 4. Schematic diagram of portion of CRTV series-contact string.

Following a CF_4/O_2 plasma treatment to remove the native oxide from the doped polysilicon surface, Ta-Si was deposited in a Varian S-Gun magnetron-sputtering system to a thickness of 1600Å. Deposition was performed in a co-sputtering mode, using a pure Ta target and two Si targets. The Ta-Si/polysilicon pattern was then defined, using CRTV mask level 1, by plasma etching in a fluorinated-gas mixture. An 875°C, 30-minute anneal in Ar reacted the Ta-Si, forming $TaSi_2$, upon which a thermal oxide was grown for 15 minutes at 720°C in steam. The interlevel dielectric, an 800Å Si_3N_4/3000Å borophosphosilicate glass (BPSG) composite, was deposited by LPCVD, and the BPSG was densified at 700°C. The interlevel contacts were then defined, using CRTV mask level 2, by plasma etching in a fluorinated-gas mixture.

Metal deposition immediately followed a dip in dilute HF to remove the native oxide from the $TaSi_2$ in the contact areas. Metal deposition was performed in a Varian S-Gun system, metal composition being either Al or Al-1%Si. The metal pattern was then defined, using CRTV mask level 3, by plasma etching in a chlorinated-gas mixture.

Metal alloying in forming gas for 30 minutes at 450°C, for improvement of the $TaSi_2$/Al contacts, completed the wafer-fabrication process sequence. After being scribed into chips, the CRTVs were ready for initial measurements and accelerated testing, the CRTV accelerated tests being performed on unpackaged chips.

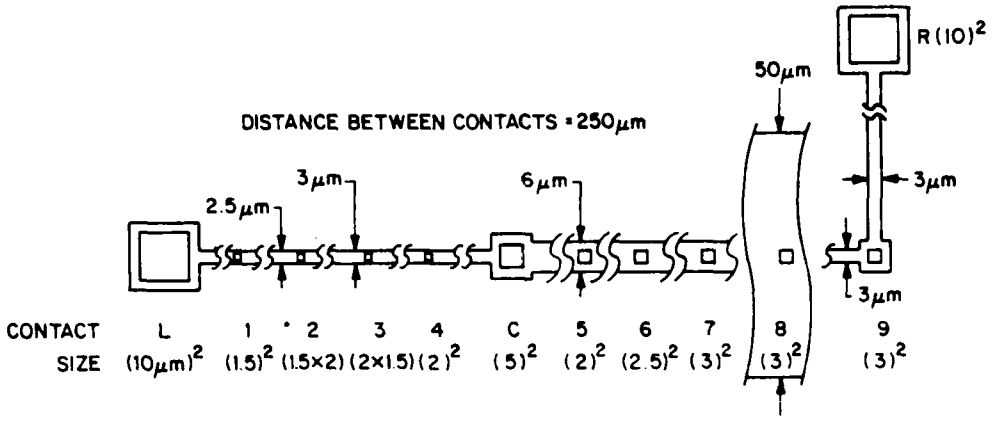


Figure 3. Schematic diagram of CRTV polycide line showing $TaSi_2$/Al contacts.

contacts. All Al lines crossing numbered contacts are of dumbbell pattern, terminating at both ends in a bond pad, thereby providing Kelvin contacts for 4-probe polycide-line-resistance, and contact-resistance measurements.

The other CRTV features relevant to this program are a contact-string structure, comprised of two-hundred 2.0 μm x 2.0 μm $TaSi_2$/Al contacts in series, and a set of six capacitors formed by 600 μm x 600 μm polycide squares, with the silicon substrate serving as counter electrode. A portion of the contact string is shown schematically in Fig. 4, with dimensions listed for polycide and Al line segments. The polycide (labelled $TaSi_2$) lies underneath the Al, but is shown shaded for clarity. Electrical contact is made to the polycide capacitors through Al bond pads routed to $TaSi_2$/Al contacts. The sizes of these contacts and the number of contacts in parallel vary from capacitor to capacitor, ranging from a single 10 μm x 10 μm contact to 1200 3 μm x 3 μm contacts.

The CRTV processing was performed at Princeton. However, processing conditions closely mirrored those used in fabricating the QMOS test circuits at SSTC. Starting with (100)-oriented silicon wafers doped with boron to ~10 ohm-cm resistivity, a 500Å gate oxide was grown in steam at 800°C, and annealed in He at 1050°C. This was followed by a low-pressure, chemical-vapor deposition (LPCVD) of 3000Å undoped amorphous silicon at 560°C, which was then doped with phosphorus from a $POCl_3$ source at 850°C.

Test and control chips were mounted in 16-pin, dual in-line ceramic (DIC) packages using Au-Si eutectic preforms. Units were then wire bonded using Al-1% Si wire, braze sealed using Au-Sn preforms, re-tested for electrical function, and given fine and gross leak checks in preparation for accelerated reliability testing.

B. CRTV CIRCUIT

The mask set for the contact-resistance test vehicle (CRTV) had been designed at RCA for investigations related to multilevel-metal-process development. As utilized in the present program, three mask levels are employed in the following sequence:

1. polycide
2. contact
3. metal,

corresponding to QMOS mask levels 4, 7, and 8, respectively, as listed in Part A of this section.

The principal features of the CRTV are a long, narrow polycide line (deposited on a 500 Å thermally-grown oxide and defined using mask level 1), with a linear array of small $TaSi_2$/metal contacts (patterned into an interlevel dielectric using mask level 2). The polycide line and contacts are shown schematically in Fig. 3. The metal (Al or Al-Si) pattern, defined by mask level 3, is omitted from the figure for simplicity. The contacts are identified either by number (1 to 9) or by letter (L, C, and R), according to their function; the larger, lettered contacts being used strictly as current taps; the smaller, numbered contacts, either as current taps and/or as the object of contact-resistance measurements.

The contact sizes are listed in Fig. 3 below the contact-number listings. They range upward in nominal size from 1.5 μm x 1.5 μm for contact 1 to 3.0 μm x 3.0 μm for contacts 7, 8, and 9. The distance between all adjacent numbered contacts is 250 μm. The nominal polycide line width is 2.5 μm between contact L and a point 125 μm to the right of contact 2, at which point it widens to 3 μm, remaining at that width up to contact C. The right side of the line from contact C to R (which was not extensively used in this investigation) includes line widths ranging from 3 μm to 50 μm. The Al (or Al-Si) lines (not shown in Fig. 3) cross the polycide line at right angles, intersecting at the

Princeton, NJ. The Ta-Si deposition processes were similar at both facilities; cosputtering in a Varian S-Gun magnetron sputtering system from separate (Ta and Si) targets to a thickness of 2000 Å with a nominal Si/Ta atomic ratio of 2.0. However, the cleaning of the polysilicon surface prior to the Ta-Si deposition differed: a dilute HF dip for the SSTC wafers, versus a CF_4/O_2 plasma treatment for the Princeton wafers (labelled LABS in Fig. 2). The polysilicon surface treatment and Ta-Si deposition were the only QMOS processes performed outside SSTC.

After deposition, the 12 test wafers were brought together for polycide anneal (30 minutes at 875°C in Ar) and re-oxidation. The polycide re-oxidation process is a 15-minute steam oxidation at 720°C. As shown in Fig. 2, this differs significantly from the standard QMOS re-oxidation process, i.e., 30 minutes in steam at 800°C. The source/drain implantations are performed after this re-oxidation, the oxide thickness over the source/drain regions during implant being 700Å in the standard QMOS process.

However, due to the lighter re-oxidation in the polycide process, the corresponding oxide thickness was only 500Å. To adjust for this, the phosphorus implant energy was lowered from the standard 110 KeV used for the control units to 90 KeV for the test units. This adjustment insured good ohmic contact in the finished test chips between the Al-Si interconnect metallization and n^+ silicon in the source/drain regions. All 18 wafers were re-combined after the source/drain implantation process.

Thirteen of the wafers survived wafer fabrication (the other five were broken). The mean circuit yield at circuit probe from the nine surviving polycide test wafers was 40.1 percent; from the five surviving polysilicon control wafers, 46.7 percent. At least one wafer from each of the six sub-splits shown in Fig. 2 had greater than 48 percent yield.

The test wafer and control wafer to provide the units for accelerated reliability testing were to be selected based on preliminary accelerated testing (thermal shock and high-current powering) on individual wafer-acceptance-test keys (WAT keys). When the results of this testing showed close wafer-to-wafer consistency, the wafers were selected based on yield and proximity to standard QMOS processing. The control and test wafers selected had yields of 70.0 percent and 65.1 percent, respectively. Both of these wafers had utilized the (standard QMOS) 1050°C $POCl_3$ doping process, the test wafer had been Ta-Si deposited at Princeton (LABS).

The first process after the split is silicon deposition for the gate electrode. It was considered advisable to split before, rather than after, this process because the standard QMOS process uses a 620°C polysilicon deposition temperature, whereas the polycide process uses a 560°C deposition temperature. The 560°C deposition yields amorphous silicon, which has a smoother surface than polysilicon [35], an advantage which could favorably influence dielectric integrity [25] and threshold stability [28] in the finished test devices.

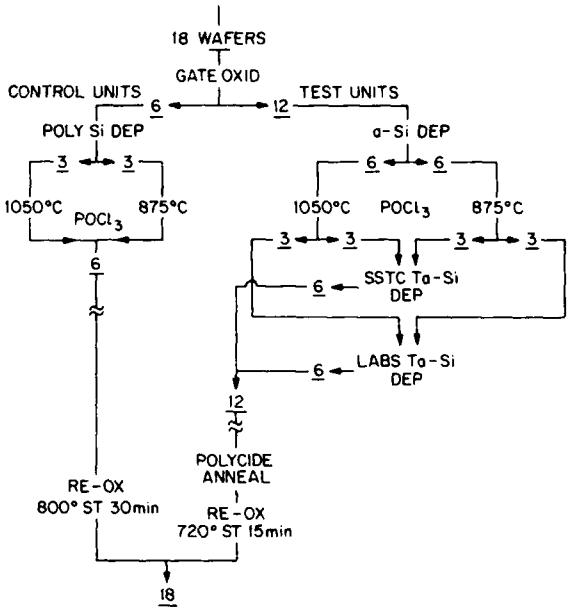


Figure 2. QMOS process flow diagram: control and test branches.

After silicon deposition, both branches are split, as shown in Fig. 2. This sub-split was prompted by another difference between the QMOS and polycide processes: standard QMOS polysilicon doping ($POCl_3$) is performed at 1050°C (which serves simultaneously as a back-side gettering step), whereas amorphous-deposited silicon for the polycide gate is doped at 875°C to minimize hillock growth on the silicon surface. Both doping processes were included in each branch to maximize the probability of realizing successful test and control wafers.

The test branch was split again for Ta-Si deposition, half of the units being deposited at SSTC, Somerville; the other half at RCA Laboratories,

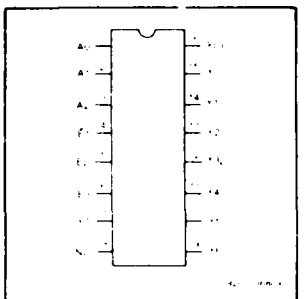
RCA
Solid State
Division

QMOS High-Speed CMOS Logic

CD54/74HC138, CD54/74HCT138
CD54/74HC238, CD54/74HCT238

Preliminary Data

File Number **1477**



TERMINAL ASSIGNMENT

3-to-8 Line Decoder/Demultiplexer Inverting and Non-Inverting

Type Features:

- *Select one of eight data output (active LOW for 138, active HIGH for 238)*
- *I/O port or memory selector*
- *3 Enable inputs to simplify cascading*
- *Typical propagation delay of 13ns @ V_{CC} 5V, 15pF, 25°C*

Family Features:

- *Fanout (Over Temperature Range)*
  Standard Outputs - 10 LSTTL Loads
  Bus Driver Outputs - 15 LSTTL Loads
- *Wide Operating Temperature Range*
  CD74HC HCT HCU 40 to 85°C
- *Balanced Propagation and Transition Times*
- *Significant Power Reduction Compared to LSTTL Logic ICs*
- *Alternate Source is Philips Signetics*
- *CD54HC CD74HC Types*
  2 to 6 V Operation
  High Noise Immunity N_{IL} 20%, N_{IH} 30% of V_{CC} @ V_{CC} 5 V
- *CD54HCT CD74HCT Types*
  4.5 to 5.5 V Operation
  Direct LSTTL Input Logic Compatibility
  V_{IL} 0.8 V Max, V_{IH} 2 V Min
  CMOS Input Compatibility
  I_{IN} 1μA @ V_{OL}, V_{OH}

The RCA-CD54/74HC138,238 and CD54/74HCT138,238 are high speed silicon gate CMOS decoders and are well suited to memory address decoding or data routing applications. Both circuits feature low power consumption usually associated with CMOS circuitry, yet have speeds comparable to low power Schottky TTL logic. Both circuits have 3 binary select inputs (A_0, A_1, and A_2). If the device is enabled, these inputs determine which one of the eight normally high outputs of the HC/HCT138 series will go low or which of the normally low outputs of the HC/HCT238 series will go high.

Two active low and one active high enables ($\overline{E}_1$, $\overline{E}_2$, and E_3) are provided to ease the cascading of decoders. The decoder's outputs can drive 10 low power Schottky TTL equivalent loads.

The CD54HC138,238 and CD54HCT138,238 are supplied in 16-lead hermetic dual-in-line ceramic packages (F suffix). The CD74HC138,238 and CD74HCT138,238 are supplied in 16-lead dual-in-line plastic packages (E suffix).

MAXIMUM RATINGS, *Absolute Maximum Values*

DC SUPPLY VOLTAGE (V_{CC})
(Voltages referenced to ground) 0.5 to +7 V
DC INPUT DIODE CURRENT (I_{IK}) FOR V_I < −0.5V or V_I > V_{CC} +0.5V) ±20 mA
DC OUTPUT DIODE CURRENT (I_{OK}) FOR V_O < −0.5V OR V_O > V_{CC} +0.5V) ±20 mA
DC DRAIN CURRENT, PER OUTPUT (I_O) FOR −0.5V < V_O < V_{CC} +0.5V) ±25 mA
DC V_{CC} OR GROUND CURRENT, PER PIN (I_{CC}) ±50 mA
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = −40 to +60°C (PACKAGE TYPE E) 500 mW
For T_A = +60 to +85°C (PACKAGE TYPE E) Derate Linearly at 8 mW/°C to 300 mW
For T_A = −55 to +100°C (PACKAGE TYPE F) 500 mW
For T_A = +100 to +125°C (PACKAGE TYPE F) Derate Linearly at 8 mW/°C to 300 mW
OPERATING TEMPERATURE RANGE (T_A):
PACKAGE TYPE F −55 to +125°C
PACKAGE TYPE E −40 to +85°C
STORAGE TEMPERATURE (T_{stg}) −65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING) FOR 10 s MAX:
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max +265°C
Under socketed or Printed Board and thickness 1.16 mm (1.59 mm)
with solder contact (not to exceed 5 s) +300°C

Figure 1. Data sheet for QMOS HC138 3-to-8 line decoder.

II. TEST-DEVICE SELECTION AND FABRICATION

A. QMOS CIRCUIT

The functional circuit for this program was selected from RCA's recently introduced high-speed CMOS logic product line (QMOS). The QMOS family incorporates 3-μm design rules with processing features which include self-aligned polysilicon gates, thin gate oxides, ion implantation, and plasma definition of contacts and conductor layers [32]. The HC138, a 3-to-8 line decoder, was selected as the specific QMOS circuit type because it had been the subject of a wide range of reliability tests [31,33], and because the complete mask set required for its fabrication was available at the RCA Solid State Technology Center (SSTC) in Somerville, NJ. Most of the QMOS fabrication and packaging for this program was carried out in a CMOS pilot line at SSTC. An objective data sheet for circuit type HC138 is shown in Fig. 1.

The QMOS wafer-fabrication process involves nine mask levels listed below in chronological sequence:

1. well
2. active area
3. P^-
4. polysilicon (control) or polycide (test)
5. P^+
6. N^+
7. contact
8. metal
9. bond pad opening

The standard QMOS process utilizes a single n^+ polysilicon layer at gate level (mask level 4, above), with contacts between the polysilicon and the overlying metal-interconnect layer. The test/control lot splits encompass processing associated with the polycide/polysilicon gate level conductor.

Eighteen wafers were carried through the wafer-fabrication process sequence with test/control splits as outlined schematically in Fig. 2. The left branch, comprising six wafers, represents the polysilicon control group; the right branch, comprising 12 wafers, represents the polycide test group.

Pursuing the approach of combining test versus control (polycide-gate) investigations on a functional circuit with specific parametric investigations on a test circuit, two different test vehicles were fabricated for this program. The functional circuit is QMOS-HC138, a 3-to-8 line decoder which is a member of RCA's recently introduced QMOS product line [31-33]. The parametric test vehicle is the Contact Resistance Test Vehicle (CRTV), the layout of which is particularly appropriate for investigations of polycide line integrity and $TaSi_2$/Al contact integrity. Both devices are described in Section II of this report.

One of the problems that had to be addressed in process development efforts had been the tendency of the polycide to peel during the annealing and oxidation processes. Peeling is, in part, induced by a high (thermally-induced) tensile stress in the silicide film at room temperature, a stress that increases with decreasing temperature [3,19]. This, together with the absence of published information on polycide survival at low temperature, prompted the choice of deep thermal cycling and thermal shock as accelerated-test modes. The QMOS circuit was the test vehicle for thermal cycling, and the CRTV, for thermal shock.

Polycide conductors will also be required to function during and after exposure to high temperatures and, in designs where the polycide is utilized for an interconnect level, to function at high current densities. Lloyd et. al. [26,27] have identified aluminum from bond pads as a participant in electromigration failure of polycide conductors. Mori et. al. [34] have shown that enhancement of electromigration failure occurs at Al/Si contacts. These considerations prompted the choice of high-temperature static-bias testing of the QMOS circuit and of high-current, high-temperature testing of the CRTV.

In Section II of this report, the QMOS and CRTV circuits are described and the processing steps used in their fabrication are outlined. In Section III, the accelerated-testing and electrical-measurement procedures used to evaluate the performance of these circuits are described. In Section IV, the results are presented and discussed, including both those from electrical measurements and those from material analysis techniques, including scanning-electron microscopy (SEM), electron-probe microanalysis (EPM), and Auger-electron spectroscopy (AES). Conclusions and recommendations for future investigations are presented in Section V.

TABLE II

Propagation delays; means and standard deviations for 4 different channels for QMOS polycide test units and polysilicon control units: pre- and post-1000 temperature cycles.

	1	2	3	4
TEST (INITIAL)	14.0 (1.44)	18.2 (1.70)	13.5 (1.39)	15.3 (1.74)
TEST (1000 CYCLES)	12.2 (1.38)	16.7 (1.84)	12.8 (1.41)	15.4 (1.74)
CONTROL (INITIAL)	22.6 (1.50)	28.2 (1.75)	21.9 (1.49)	24.6 (1.59)
CONTROL (1000 CYCLES)	20.7 (1.53)	26.6 (1.63)	21.2 (1.55)	24.6 (1.57)

decreases. The post-250°C statistics on the control group represent 24 units while those on the test group, like the initial statistics, represent all 27 units.

As the first step in failure analysis, a slow voltage ramp was applied to the input of the failed polycide gate unit. When a short occurred at 10 V, the unit's lid was removed and the failure site located. The failure site is shown in Fig. 6, in which part (a) is a 1000X photomicrograph and part (b) is a schematic drawing identifying the relevant features in the photomicrograph.

The failure site is under a p-channel gate, and the failure was due to increased leakage across the gate oxide (which subsequently shorted upon application of the voltage ramp). Running diagonally across and under the source metal and gate is a scratch which is visible only in areas not covered by the gate or metal. The scratch evidently occurred before gate deposition, locally decreasing the gate-oxide thickness and increasing its susceptibility to leakage and breakdown. It is therefore concluded that the scratch rather

TABLE III

N-channel and P-channel threshold distributions, QMOS polycide test units and polysilicon control units: pre- and post-bias life testing.

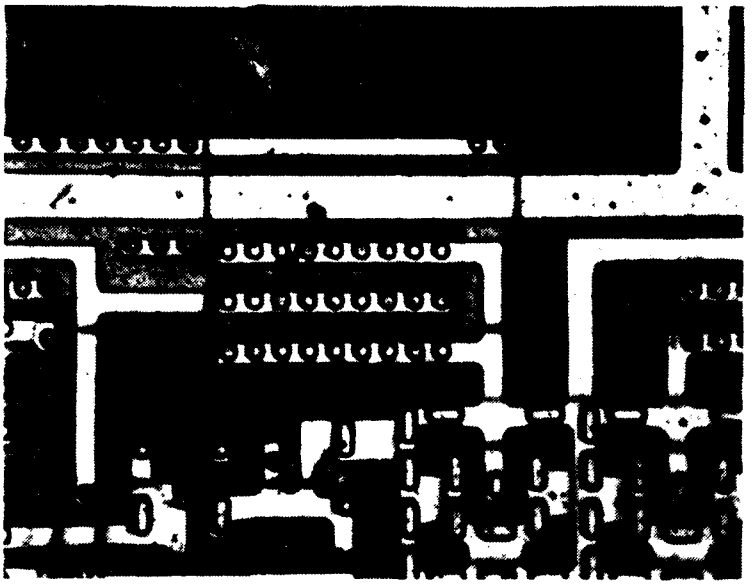
	N-CHANNEL TRANSISTORS		
THRESHOLD VOLTAGE (V)	0.76	0.80	0.84
TEST (INITIAL)	1	20	6
TEST (POST 250°C)	6	17	4
CONTROL (INITIAL)	3	23	1
CONTROL (POST 250°C)	5	18	1

	P-CHANNEL TRANSISTORS						
THRESHOLD VOLTAGE (V)	1.08	1.12	1.16	1.20	1.24	1.28	1.32
TEST (INITIAL)	1	7	14	5			
TEST (POST 250°C)		5	13	9			
CONTROL (INITIAL)			1	2	20	4	
CONTROL (POST 250°C)				1	1	18	4

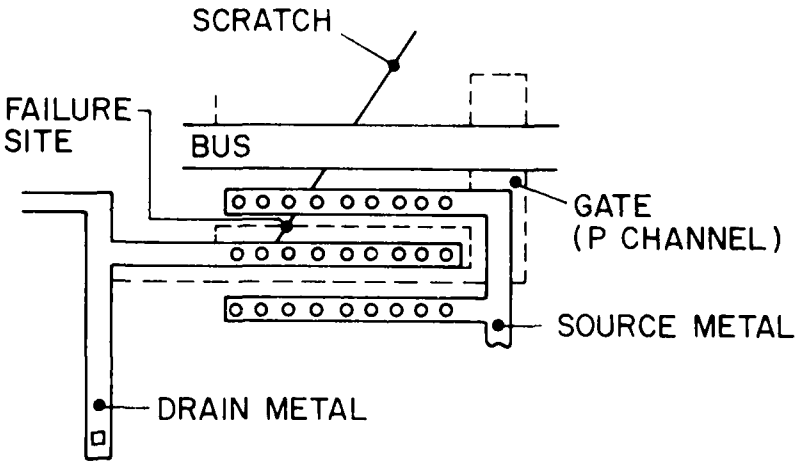
TABLE IV

Propagation delays; means and standard deviations for 4 different channels for QMOS polycide test units and polysilicon control units: pre- and post-bias life testing.

	1	2	3	4
TEST (INITIAL)	13.5 (1.06)	17.8 (1.36)	13.2 (1.01)	14.6 (1.34)
TEST (POST 250°C)	12.2 (1.06)	15.9 (1.41)	13.1 (1.04)	14.6 (1.38)
CONTROL (INITIAL)	22.9 (0.51)	28.6 (0.65)	22.2 (0.46)	25.0 (0.50)
CONTROL (POST 250°C)	21.4 (0.52)	26.6 (0.72)	22.3 (0.47)	25.1 (0.68)



(a)



(b)

Figure 6. Photomicrograph of failure site and vicinity on QMOS test unit (1000X) and schematic drawing of same area.

than any property of the overlying polycide gate was the cause for this single polycide-unit failure.

B. CRTV CIRCUIT

1. Thermal Shock

a. Gate-Oxide Integrity.

Koburger et. al. [25] have shown that a polysilicon-layer thickness of at least 2000Å was required in a polycide composite to assure good integrity of the underlying gate oxide. The polysilicon thickness in our units was 3000Å, and previous experiments at RCA [39] have shown the oxide integrity under unshocked $TaSi_2$-polycide gates to be the approximate statistical equivalent of that under polysilicon gate electrodes. With this background, the objective of the present experiment was to determine the effect of thermal shock on polycide-gate units. Consequently, the test/control groups comprised shocked/unshocked units, both with polycide gates.

No significant dependence of oxide breakdown voltage on the number or size of $TaSi_2$/Al contacts was observed; therefore the capacitor-breakdown results were combined in a single cumulative distribution plot. These results are given in Fig. 7, in which the cumulative percent of capacitor breakdown failures at $V = V_o$ is plotted versus V_o for unshocked units, and for units which had experienced 30 cycles of thermal shock. The sample sizes were 36 shocked units and 42 unshocked units, test/control chips being from adjacent rows on the same wafer. Both sets of capacitors show a broad distribution with approximately 15 percent shorted capacitors. However, the distributions are very similar in all features. It is thus concluded that thermal shock did not undermine gate-oxide integrity in these units. It is noted that the unusually large size of these capacitors (600 μm x 600 μm) provided a severe test of the effects of stress induced by mismatches in thermal-expansion coefficients. This could account for the broad voltage-breakdown distributions.

b. Polycide Line Integrity.

Initial, periodic, and post-30-cycle polycide-line voltage measurements were performed in test-mode 1 (see Fig. 5) in this experiment. This measurement, which was performed at a test current of 1mA, provided four-probe determination of the resistances of polycide line-segments 1-2 and 3-4, and two-probe determination of the terminal resistance, which is the sum of the

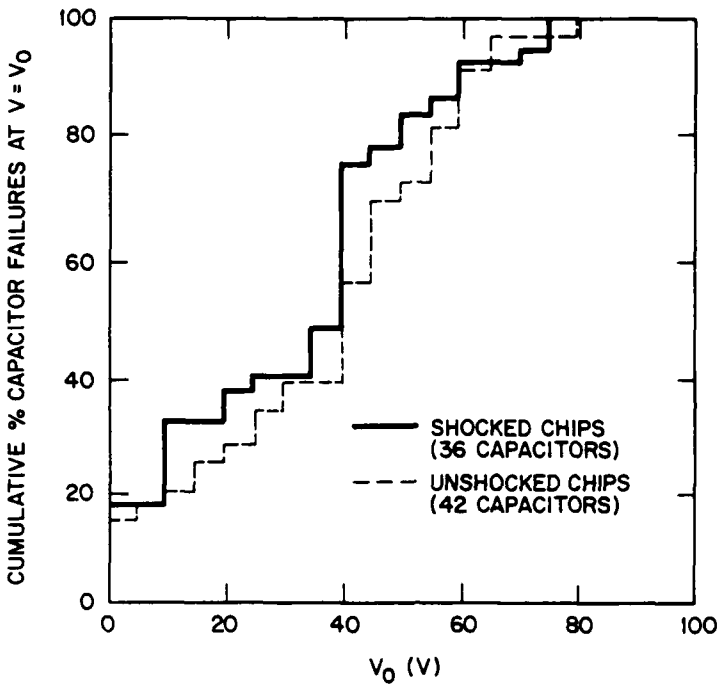


Figure 7. Cumulative gate-breakdown-voltage failure distibution plots for thermally shocked and unshocked CRTV polycide capacitors with a 500 Å steam-grown gate oxide.

entire polycide line resistance and the contact resistances at the two large end contacts, L and R. (These contact resistances, while not separately measurable, are almost certainly below 1 ohm because of the large size of contacts L and R.)

Initial measurements showed chip-to-chip and wafer-to-wafer distributions of polycide sheet resistivity to be narrow, within approximately ± 10 percent. Typical values were V_{12} = 0.275V, V_{34} = 0.225V, and V_{LR} = 2.31V, where V_{12}, V_{34}, and V_{LR} are the voltages between contacts 1 and 2, contacts 3 and 4, and the (L and R) end terminals, respectively. These values translate to resistances of 275 ohms, 225 ohms, and 2310 ohms, respectively, and to sheet resistances of approximately 2.8 ohms per square for both line segment 1-2, which is 250 μm long and 2.5 μm wide (100 squares), and line segment 3-4, which is 250 μm long and 3.0 μm wide (83 squares). Films thickness being approximately 1600Å, this corresponds to a $TaSi_2$ resistivity of 4.4×10^{-5} ohm-cm. (In this resistivity calculation the contribution of the polysilicon, the sheet resistance of which had been measured in-process to be greater than 40 ohms per square, was neglected.)

Measurements of polycide line resistance after 1, 5, 13 and 30 thermal-shock cycles all showed less than 1 percent change from initial values.

c. Other Tests.

Several units from the thermal shock tests were subjected to high-current testing, as will be discussed in detail in Section IV-B2, below.

2. High-Current Testing

The principal test modes for the high-current tests were modes 2, 4, 5, 6 and 7, the electrical connections for which were described in conjunction with Fig. 5.

a. Test Mode 2.

The mode-2 electrical hookup, shown as part of Fig. 5, is re-drawn for convenient reference in Fig. 8. Current is drawn along the polycide line between contact L, which was the positive contact for all units tested, and contact 3, with current flowing past contacts 1 and 2 which provide voltmeter taps for four-probe line-resistance measurement of the 2.5 μm wide segment 1-2. Contact resistance at contact 3 is calculated from the voltage V_{34} measured between contact 3 and contact 4. The above measurement features, together with a large end contact (L) in conjunction with a small end contact (3) and a narrowing of the polycide linewidth from 3 μm to 2.5 μm (between contacts 2 and 3), made the mode-2 configuration a promising one for a determination of the relative failure probabilities of the various features associated with the polycide line.

Eighteen Al-1%Si metallized chips and 13 Al-metallized chips were subjected to 10-minute-increment, mode-2 testing to failure at room-temperature ambient. Fig. 9 shows the mean temperature of polycide line 1-2, calculated from in-situ line resistance measurements and the $TaSi_2$ TCR, plotted versus time for four different powering currents; 30, 40, 50, and 60mA. The first in-situ measurement (zero time on Fig. 9) is made approximately 1 second after current is applied.

From the near-zero curve slopes at 30, 40, and 50mA, it is seen that the line temperature comes to equilibrium very rapidly, 95 percent of the 10-minute temperature rise occurring within this first second. Only at the 60mA current is there a significant increase with time after 1 second, a harbinger of the

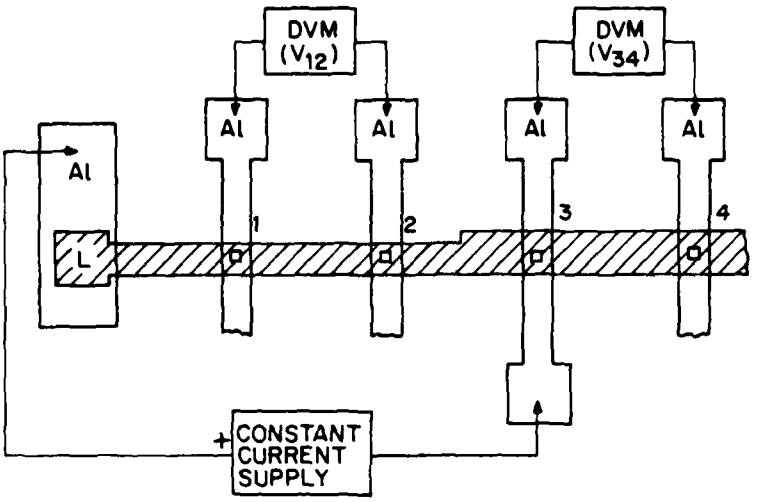


Figure 8. Schematic diagram of CRTV mode-2 electrical connections.

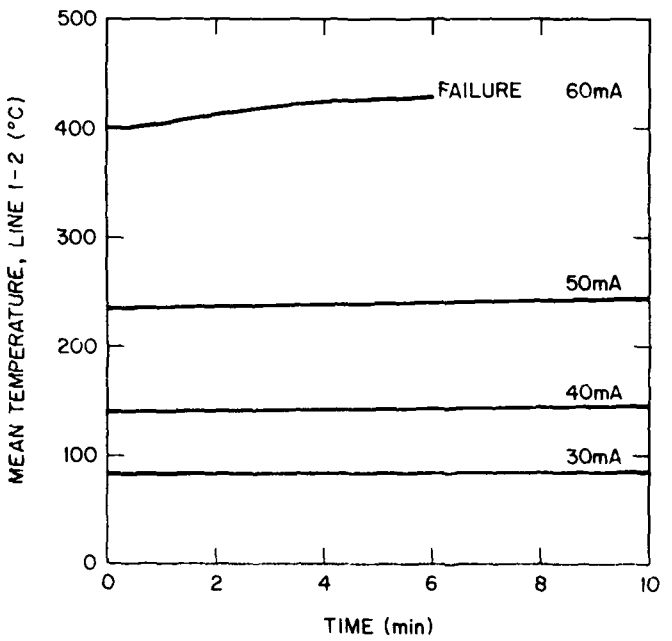


Figure 9. Mean temperature of CRTV line segment 1-2 versus time during 10-minute mode-2 testing increments at the currents as labelled.

catastrophic failure which occurred between the 6- and 7-minute readings at this current.

In Fig. 10, the mean temperature of line-segment 1-2 is plotted versus current for the 13 Al-metallized units. Temperatures for 12 of these 13

units fall within a very narrow envelope, indicating good consistency in the units response to powering. Line resistance measurements yielded consistent results for both Al- and Al-1%Si metallized units, in-situ curves increasing with time and current as typified by Figs. 9 and 10, respectively; whereas resistances measured at 1mA between power increments remained constant at their pre-powering values right up until failure.

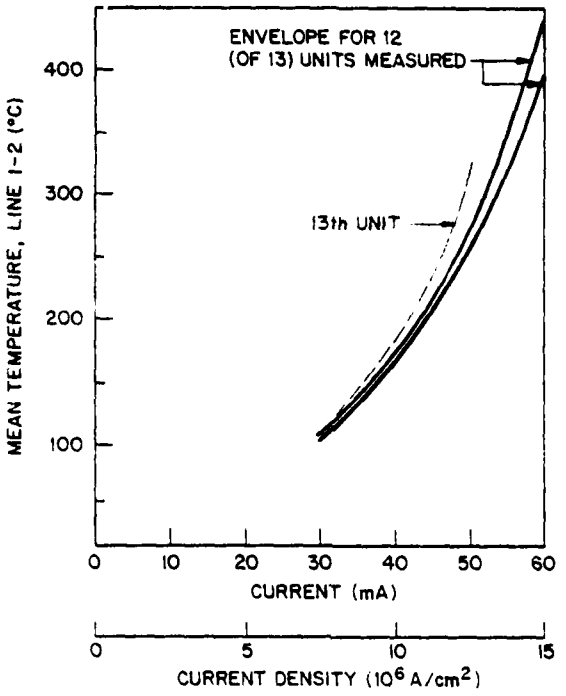


Figure 10. Mean temperature of CRTV line segment 1-2 versus current and current density for 13 units during 10-minute mode-2 testing.

The contact resistances were not as consistent. An example of a set of in-situ measurements of contact resistance is shown in Fig. 11, in which the contact resistance at contact 3 is plotted on logarithmic scale versus current for an Al-metallized unit. In addition to the level-to-level increases, which could imply a temperature coefficient of contact resistance, there were often precipitous jumps (shown as the vertical lines with arrows in Fig. 11) during the 10-minute powering increments at currents as low as 40mA. Such jumps were absent from the line-resistance curves except near the onset of catastrophic failure.

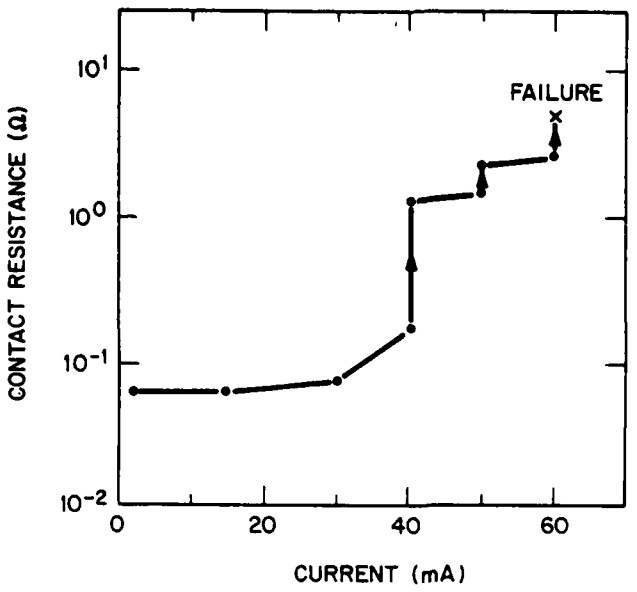


Figure 11. Contact resistance of contact 3 versus current for a unit which experienced contact degradation during 10-minute mode-2 testing.

It was decided that these jumps would not be considered failures for the purpose of this experiment. The reasons for this decision were that the jumps were relatively small (< 2 ohms, the equivalent of less than one square of polycide) and that the contact-resistance values measured at 1mA after such jumps were usually equal to the initial 1mA values.

The criteria adopted to define failure in this experiment were (1) a greater than 15 percent increase in line resistance at 1mA and/or (2) a greater than 5 ohm increase in contact resistance at 1mA, both measured with respect to the initial values. In practice, the 10-minute-increment testing always resulted in more catastrophic failures, usually in open lines and/or contacts.

Figure 12 gives cumulative distributions of polycide failure temperature, showing the cumulative percent of polycide failures at $T = T_o$ plotted versus T_o. The temperature measurement used to derive this curve is that calculated from the last pre-failure in-situ measurement, e.g., the 6-minute, 60mA reading in Fig. 9. Since readings were made only on the minute, T_o is more accurately the average line temperature within 1 minute of failure.

The distribution for Al metallized units is remarkably narrow, ranging from 360°C to 429°C, with a mean value of 416°C and a standard deviation of

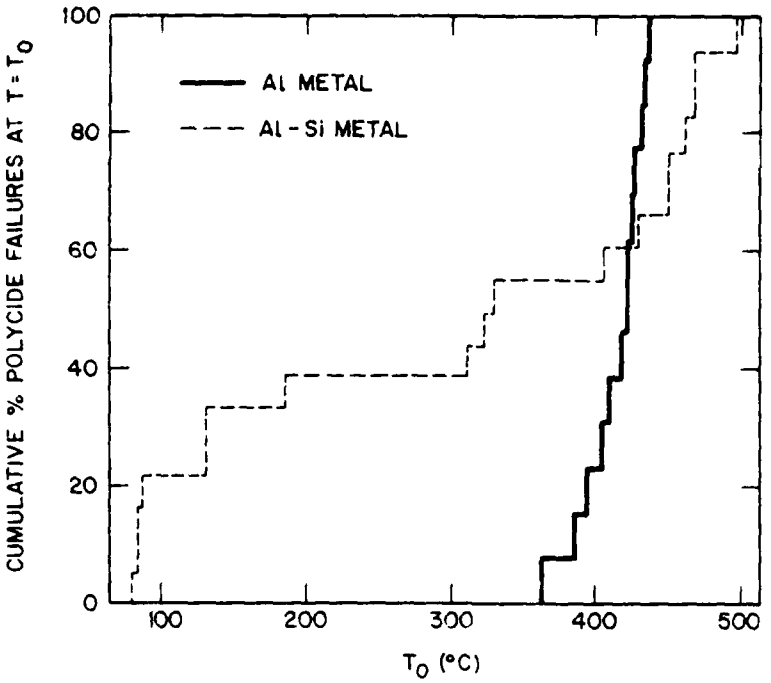


Figure 12. Cumulative polycide-line failure distribution plots versus mean line-segment temperature for Al- and Al-Si metallized units under 10-minute testing in mode 2.

19.7°C. Four of these 13 units had undergone the thermal-shock test prior to mode-2 testing. The failure temperature for these four units were 393°C, 403°C, 421°C, and 424°C, well within the distribution. This suggests that thermal shock does not weaken the units' power capabilities.

In contrast to the distribution for Al-metallized units, the failure-temperature distribution shown for Al-1%Si metallized units in Fig. 12 is very broad. However, this distribution can be broken into three distinct branches; (1) an "early failure" branch, consisting of seven units, in which failure occurred below 200°C; (2) an "intermediate" branch, consisting of three units, in which failure occurred between 300°C and 325°C; and (3) a "mainstream" branch, consisting of eight units, in which failure occurred between 400°C and 500°C. The mainstream branch is reasonably consistent with the entire distribution for the Al-metallized units, although somewhat higher in mean temperature (457°C), and standard deviation (29.1°C).

Failure sites were determined on all failed units by optical-microscope examinations, and photomicrographs of all failure sites were made. Typical photographs for mainstream (>400°C) failures are shown in Figs. 13 through 16.

Figures 13 and 14 were taken at 500X magnification, Fig. 13 on an Al-metallized chip, Fig. 14 on an Al-1%Si metallized chip. Contact L is at the left-center; contact 1, at the right-center in both photos. The Al (Al-Si) bus extends upward from contact L; the Al (Al-Si) interconnect extends vertically in both directions across contact 1. In Fig. 13, the damaged area of the polycide line extends from contact L to approximately 20 μm past contact 1; in Figure 14, the damaged area extends from contact 1 to the left for approximately 160 μm and to the right for approximately 5 μm.

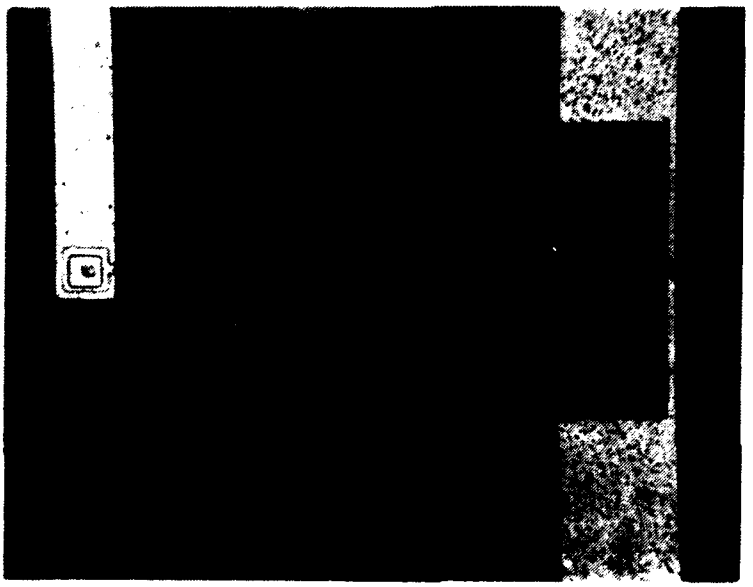


Figure 13. Photomicrograph of failure site in Al-metallized, mode-2 mainstream failure: contact L, contact 1, and vicinity at 500X magnification.

Multiple (unconnected) failure sites were not uncommon; this is illustrated in Fig. 15, taken at 1000X magnification, which shows contact 3 and vicinity for the same chip pictured in Fig. 14. The damaged area here extends from contact 3 to the left for a distance of approximately 50 μm. It is noteworthy that in all mode-2 failures, all damage sites were associated with a contact. There were no failures along isolated sections of the polycide lines. This suggests that the weak link in this materials composite is not the polycide line, but rather the $TaSi_2$/Al (or Al-Si) contacts.

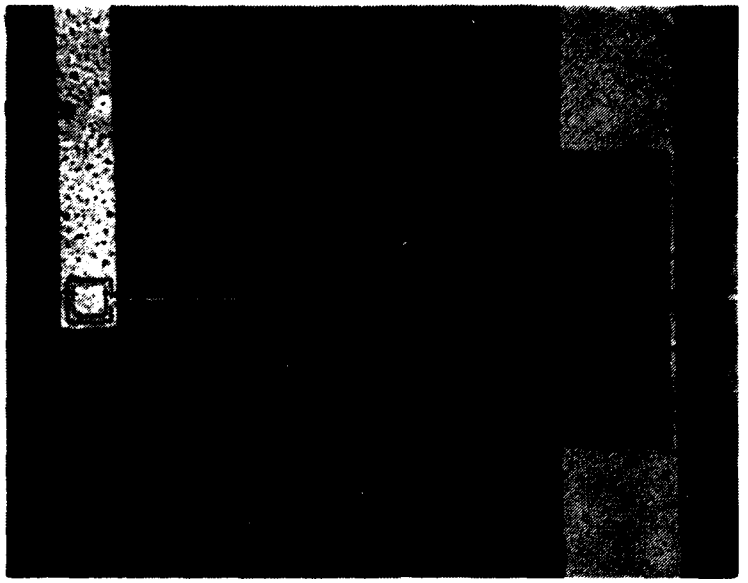


Figure 14. Photomicrograph of failure site in Al-1%Si metallized, mode-2 mainstream failure: contact L, contact 1, and vicinity at 500X magnification.

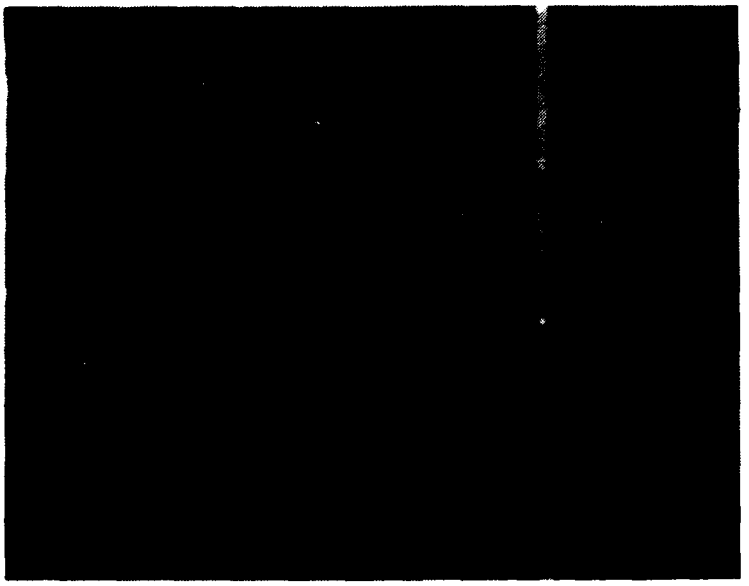


Figure 15. Photomicrograph of a second failure site on same unit as shown in Figure 14: contact 3 and vicinity at 1000X magnification.

Figure 16. Photomicrograph of failure site in Al-1%Si metallized, mode-2 mainstream failure: contact L, contact 1, and vicinity at 500X magnification, showing gross melting at Al-1%Si interconnect at failure site.

Several failure sites showed signs of gross Al or Al-Si melting as illustrated in Fig. 16. Clearly, in such instances the local temperature at failure had risen to at least 660°C, the melting point of Al. This points up a difficulty in the interpretation of the average line temperature, as illustrated in Fig. 17, which gives speculative plots of the temperature distribution along the length of polycide line segment 1-2. Curve A represents the probable shape of the distribution for an as-yet undamaged situation, in which the current is 60mA and the average line temperature is calculated to be 400°C. The peak temperature is above 400°C, and is located at the midpoint between contacts 1 and 2 while the contact temperatures are less than 400°C. Curve B shows the presumed situation after the start of degradation at contact 1, at the start of a local temperature avalanche. Curves C and D show the progressive development of this temperature spike, with failure finally occurring, accompanied by Al melting (curve E).

Figures 18 and 19 show 1000X failure-site photographs for two chips experiencing early failures. In contrast with the mainstream failures, all of which included at least one internal contact as a failure site, the only failure site in each of the seven early failures was contact 3, the (negative)

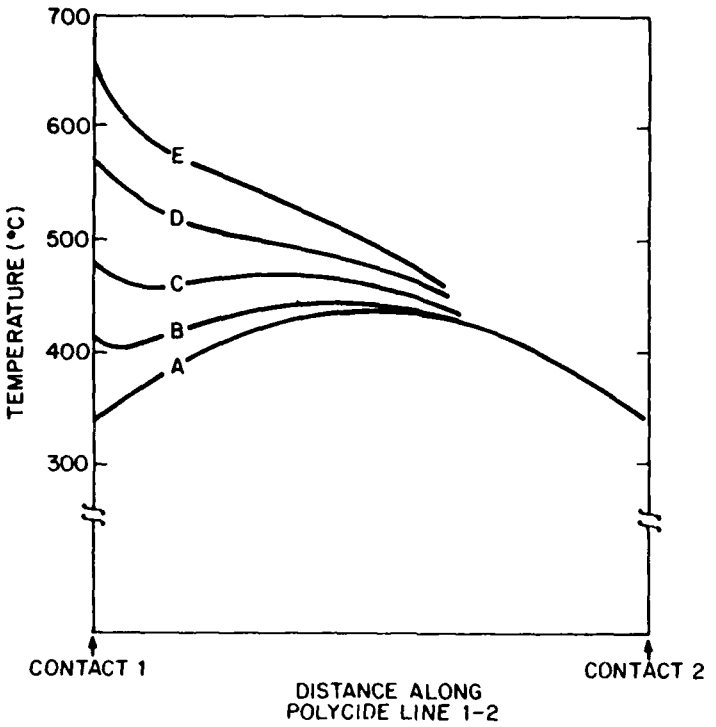


Figure 17. Speculative temperature distribution along line segment 1-2 during powering for undamaged line (curve A), and during the thermal runaway process leading to failure and Al melting at contact 1 (curves B to E).

end contact. This, together with the cause for the early failures, is illustrated in Fig. 20, in which the current density at failure is plotted versus the initial contact resistance measured at contact 3. Approximate failure temperature is plotted on the right-side ordinate for reference. All Al- and Al-1%Si metallized units are represented, with no specific distinction being made between the two types.

However, a very clear distinction is evident between the (early, intermediate, and mainstream) failure groups, the distinction being in initial contact resistance (abscissa) as well as in failure level (ordinate). All seven members of the early-failure group had initial contact resistances of greater than 3 ohms. Subsequently, all failed at current densities below 1 x 10^7 A/cm^2. In contrast, all 21 mainstream units had initial contact resistances below 1.1 ohms, and all failed at 1.4 x 10^7 A/cm^2 or above. All three intermediate-group members failed at 1.3 x 10^7 A/cm^2, and although all had failure sites at contact 3, two of these chips had an additional failure site.

d. Test Mode 7.

Up to this point, all CRTV high-current-test failures had involved a $TaSi_2$/Al (or Al-Si) contact; there were no isolated polycide-line failures. Mode 7 represented a final attempt to cause such failures. This attempt involved making the weaker contact by polarity, i.e., the positively biased contact, very large. The electrical hookup, as shown in Fig. 5, has current flowing between contact 4 and contact C. All mode-7 tests were performed in negative (-) polarity, i.e., with contact C (5 μm x 5 μm) being the positive contact.

Four Al-metallized units were subjected to 10-minute-increment tests in this mode. Three units failed at a current density of 1.9×10^7 A/cm^2; the fourth, at 2.0×10^7 A/cm^2. A 760X photograph of one of these units is shown in Fig. 29, in which the damaged area is near the left side of the photo, whereas contact C, near the right, and the Al line extending upward to C appear to be undamaged. This is the only unit in which an isolated polycide-line failure is visually suggested.

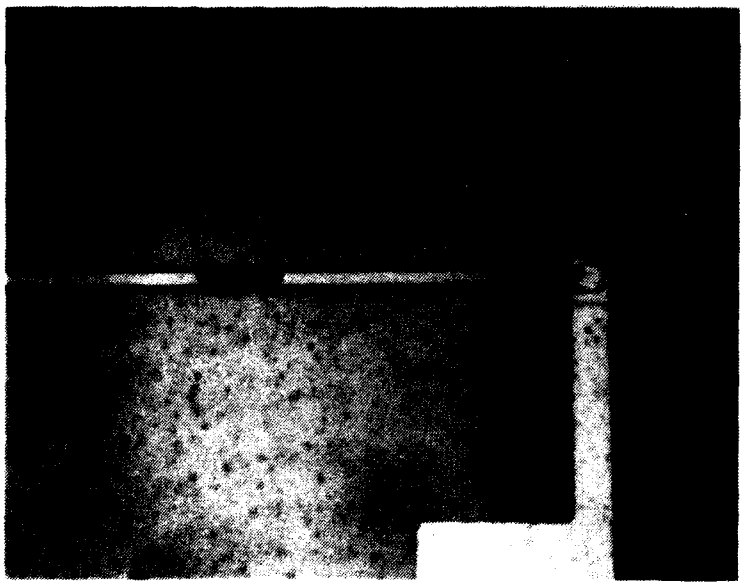


Figure 29. Photomicrograph of failure site in Al-metallized mode-7 failure: contact C and vicinity at 760X magnification.

Another failure in this mode, shown at 500X magnification in Fig. 30, provides an interesting contrast. Figure 30 shows an area along the polycide line

inutes (16 hours) and then removed for material analysis; the ninth survived 400 minutes (40 hours) of powering. Seven additional Al-metallized units were owered at 1.2 x 10^7 A/cm^2 for 64 hours; no failures occuring in this group.

Temperature versus time plots for the units failing after 250 minutes and 200 minutes at 1.5 x 10^7 A/cm^2 are shown in Fig. 28. Measurements were made t 10-minute intervals, and it is seen that most of the increase in mean line emperature occurred in the first 100 minutes. Temperatures at the last eading before failure were 347°C (620°K) and 342°C (614°K).

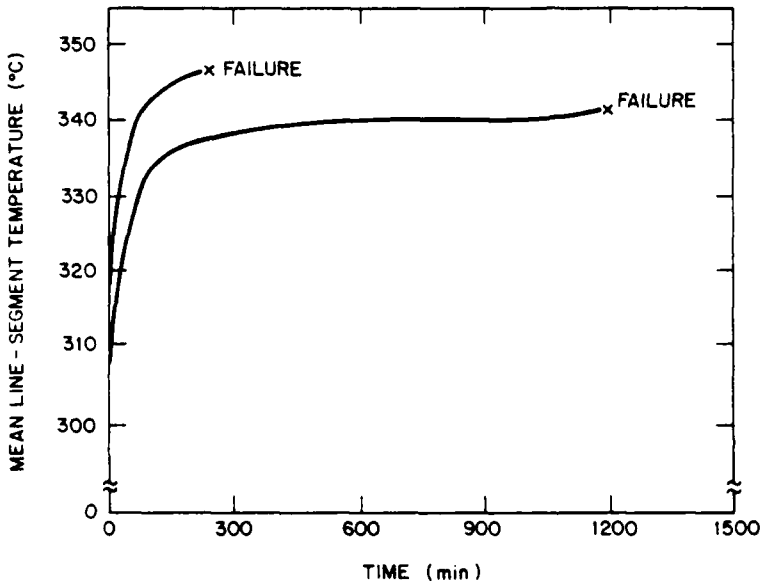


Figure 28. Mean temperature of line segment 1-2 versus time for two CRTV units powered to failure at a current density of 1.5 x 10^7 A/cm^2 in mode 6.

Roughly speaking, comparison between the 10-minute-increment and constant-urrent results suggest a two-orders-of-magnitude (∿100 times) increase in time o failure with a ∿150 C decrease in mean line temperature (from approximately 70 K to 620 K). An Arrhenius calculation using these values results in an ctivation energy of ∿1.3 eV, a value to be interpreted with all of the kepticism attendant to the limitations of the experiment.

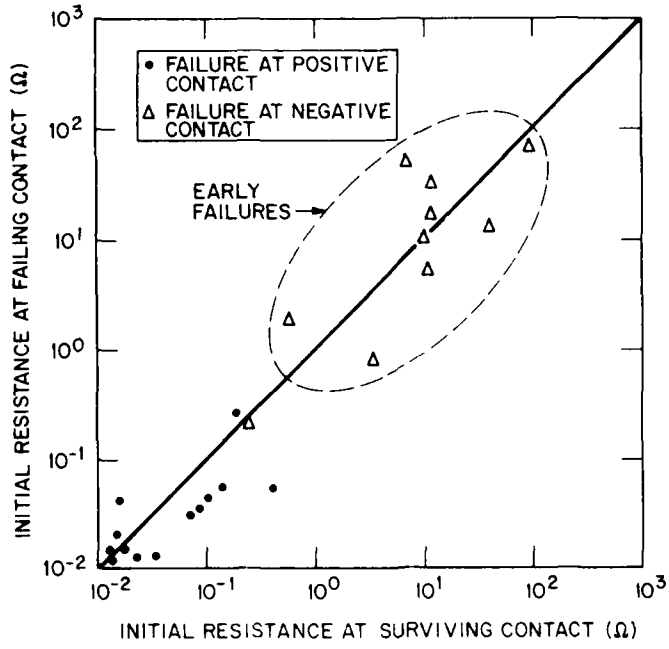


Figure 27. Logarithmic plot of initial contact resistance at failing contact (in mode-5 or mode-6 testing) versus initial contact resistance at surviving contact. Diagonal line at 45° is line of equality of these two resistances.

Several Al-metallized units were subjected to longer-term powering at current levels slightly below the failure levels determined in 10-minute-increment testing. Some of these units were removed from the tests before failure to provide heavily-powered, but unfailed samples for SEM, EPM and AES material analyses. Others were tested to failure to obtain a rough idea of activation energies for high-current/high-temperature failure.

In this context it is pointed out that the combination of (relatively) high sheet resistance and very high current-density capability of the polycide line make it virtually impossible to vary the line temperature and current density independently. Consequently, it is very difficult to determine clear-cut activation energies for failure in the manner analogous to those determined for electromigration failure in Al lines [40].

Twelve Al-metallized units were powered at 1.5×10^{7} A/cm^{2} for extended times. Only three of these units experienced failure, these occuring at times of 250 minutes, 1110 minutes, and 1200 minutes. All three failures were at the positive contact. Eight of the nine surviving units were powered for 960

For a given current, line-segment 1-2 is significantly hotter under mode-2 powering than under mode-6 powering, as expected given the different current-endpoint conditions. Mean line-segment temperature at failure was also higher in modes 5 and 6, averaging approximately 500°C for mainstream failures, as compared with 416°C in mode 2. This difference is undoubtedly due to differing temperature distributions, temperature gradients along the line being higher in modes 5 and 6.

Another striking feature of the failure data shown in Fig. 24 is a strong polarity effect, all of the early failures occuring at the negatively-biased contact, while all except one of the mainstream failures occur at the positive contact. This result was independent of the (±) biasing polarity of the external circuit, and of the metallization type. Within any single chip both mode-5 (or -6) contacts were found to belong in the same grouping, i.e., no unit was found with contact 3 having << 1 ohm resistance and contact 4 having >> 1 ohm resistance.

This is illustrated in Fig. 27, a logarithmic plot in which both ordinate and abscissa represent initial contact resistances; the ordinate, that of the contact at which failure eventually occurs; the abscissa, that of the surviving contact. All of the early failures are seen to fall into the upper-right quadrant of this figure; all of the mainstream failures, into the lower left.

This segregation of failure groups, together with that shown in Figs. 20 and 24, suggests the expectation that in a contact pair, the one with the higher initial resistance will be the weaker of the pair, and will therefore be the one which fails. However, close examination of Fig. 27 shows this not to be the case. Only those data points which lie above and to the left of the 45-degree line represent units in which the contact with higher initial resistance failed, and less than half of the points fall inside this region. Evidently, within a given failure group, the contact's polarity is a stronger determining factor than initial contact resistance. However, pre-failure degradation in the mainstream-failure group was not unipolar, contact-resistance increases similar to those shown in Fig. 11 being measured at both positive and negative contacts.

The overall polarity behavior exhibited in the results shown in Figs. 20, 24, and 27 is rather complex. Coupled with complexities previously reported [26], these results indicate the need for additional investigations into polarity effects in polycide conductors and polycide/metal interfaces under electromigration-type stressing.

Figure 25. Photomicrograph of Al-1%Si metallized CRTV in which the Al-Si interconnect has been stripped, but in which the interconnect pattern is still visible as Si precipitates (freckles) on interlevel dielectric surface: contacts L, 1, and 2 and vicinity at 200X magnification.

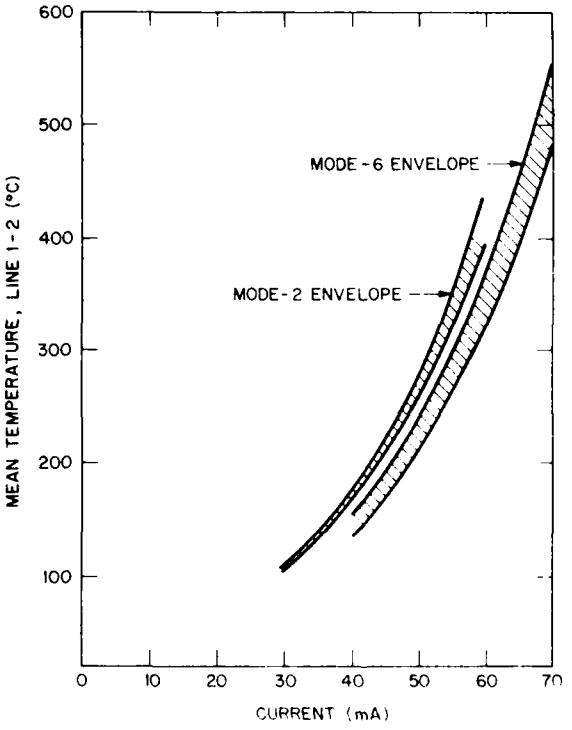


Figure 26. Mean line temperature of CRTV line segment 1-2 versus current for units during 10-minute mode-6 testing, with corresponding mode-2 envelope repeated from Figure 10 for comparison.

Thus, the results demonstrate consistently that an initial contact resistance of greater than 1 ohm at the $TaSi_2$/Al-Si interface would constitute a severe weak link in VLSI circuits designed for substantial interlevel currents. This points up the necessity of exercising special care in the process steps which determine the quality of the $TaSi_2$/Al-Si contact, i.e., interlevel-dielectric etch, photoresist strip, dilute-HF contact-cleaning dip (or in-situ cleaning), and Al-Si deposition.

Detection is also a problem, the 1 ohm threshold for loss of contact integrity representing the resistance equivalent of less than one square of polycide. Such an additional resistance would go totally undetected in both static and dynamic WAT-key and circuit-probe testing unless special test structures which isolate and measure individual contacts (not contact strings) are utilized. This points up the necessity of including test structures, such as that shown in Fig. 23, on the WAT keys at the minimum, and, preferably, both on the WAT keys and on the individual circuits.

The reason for the high resistances in some of the contacts on Al-1%Si metallized units is believed to be related to the presence of silicon precipitates (from the Al-Si alloy) at the contact interface. It has been shown previously that such precipitates interfere with the formation of good ohmic contacts when the contact interface is not entirely clean [38]. The presence of such precipitates (often called freckles) was clearly observed on the interlevel-dielectric surfaces of these chips upon stripping the Al-1%Si film.

The precipitate pattern is so dramatically visible in Fig. 25, a 200X photo of the vicinity around contacts 1 and 2, that the image of the (stripped) Al-Si interconnect pattern can still be seen. The visibility of the precipitates on the dielectric surfaces is due to the smoothness of the latter.

In contrast, the $TaSi_2$ is polycrystalline as are the silicon precipitates. Consequently, it was not possible to clearly distinguish silicon precipitates in the contact areas by either optical or SEM inspection, and thus, it was not possible to visually distinguish between good (< 1 ohm) and bad (> 1 ohm) contacts.

The mainstream failures for modes 5 and 6 shown in Fig. 24 were at polycide-line current densities ranging from 1.6×10^7 to 1.8×10^7 A/cm^2, higher than the corresponding range for mode-2 mainstream failures shown in Fig. 20, i.e., 1.4×10^7 to 1.6×10^7 A/cm^2. The explanation for this is shown in Fig. 26, where the envelope of mean temperatures of line-segment 1-2 is plotted versus current for six units powered in mode 6, together with the corresponding envelope for the same line segment powered in mode 2 (the latter reproduced from Fig. 10).

However, the line-segment voltage V_{12} in this hookup includes the voltages across both contacts. Consequently, it was necessary to substract V_{L1} and V_{23} from V_{12} in the calculation of the polycide line-segment resistance. Also, since neither mode 5 nor mode 6 was completely symmetrical (contact 4 being larger than contact 3, and contact 2 being larger than contact 1), polarity effects were tested by running approximately half of the units in reverse-bias (-) polarity.

Ten minute-increment mode-5 and -6 tests to failure were performed on 14 Al-Si metallized units and 10 Al-metallized units. Results of these tests are shown in Fig. 24, where the current density at failure is plotted versus the initial contact resistance of the contact at which the eventual failure occurred. Similar to the case shown in Fig. 20 for mode-2 failures, the results in Fig. 24 fall into distinct categories; units with high initial contact resistance (> 1 ohm) which experience early failure (< 1.2 x 10^7 A/cm^2); and units with low initial contact resistance, which experience "mainstream" failures with a narrow distribution between 1.6 x 10^7 A/cm^2 and 1.8 x 10^7 A/cm^2.

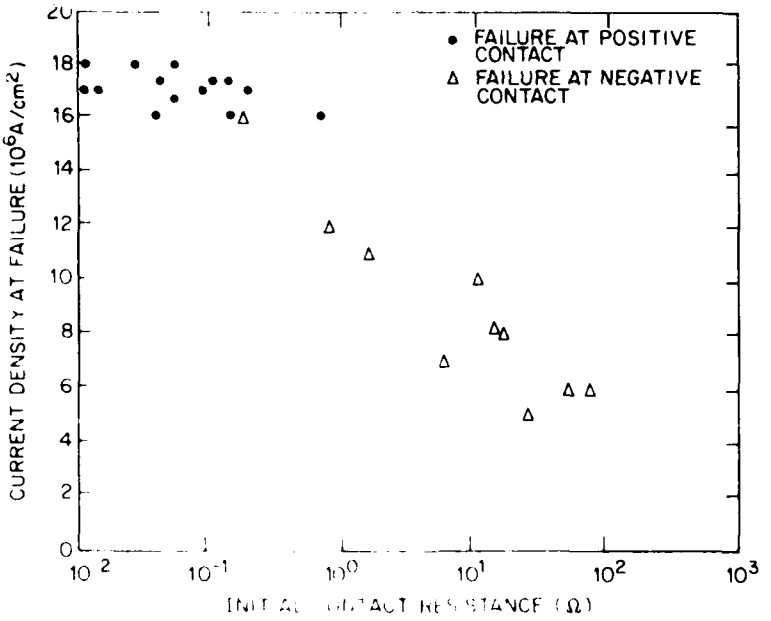


Figure 24. Current density at failure versus the initial contact resistance of the contact which eventually experiences failure in mode-5 and -6 tests. Open circles indicate failures at negative contact, and solid circles are failures at positive contact.

The predominance of contact 2 as a failure site is therefore due to the combined effect of its internal location and larger heat dissipation in the (narrower) underlying polycide line.

c. Test Modes 5 and 6.

Modes 5 and 6 were very similar, the current path in the former being from contact 3 to contact 4; in the latter, from contact 1 to contact 2. The important differences were the larger contact sizes and line width in mode 5 (see Fig. 3). These differences were accounted for, in combining the results of the two modes, by dividing the failure current by the polycide line cross section, i.e., by calculating and plotting the results in terms of polycide-line current density.

The reasons for testing in modes 5 and 6 were (1) to eliminate the complication of internal contacts and (2) to test for polarity effects. As illustrated in Fig. 23, a schematic of the mode-6 electrical hookup, contact L and contact 3 act as auxiliary voltage taps for V_{L1} and V_{23}, respectively, from which measurements the contact resistances at contact 1 and contact 2, respectively, are calculated.

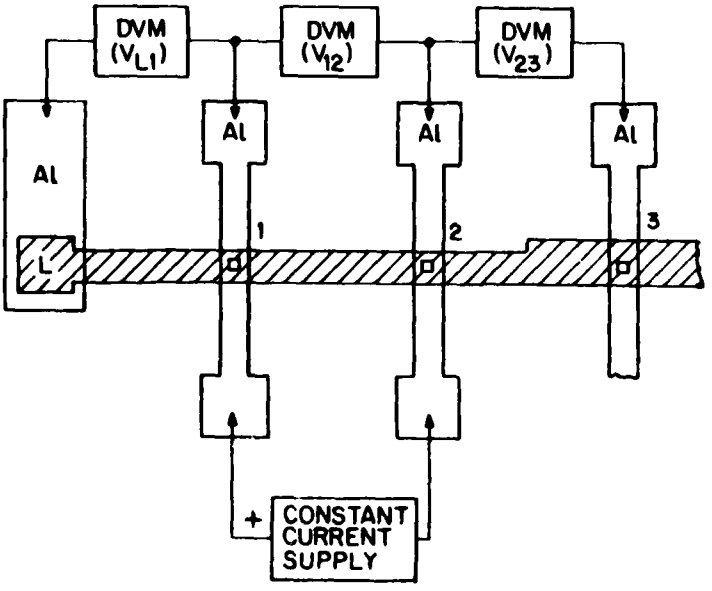


Figure 23. Schematic diagram of CRTV mode-6 electrical connections.

of these units, contact 1 had the highest resistance (30 to 1000 ohms); in the sixth, contact 2 had the highest resistance (400 ohms). Thus, as in the room-ambient tests, contact 1 (and vicinity) was the predominant failure site.

All subsequent test modes (modes 4 to 7) were performed at 25°C ambient because it resulted in more-readily identifiable failure sites.

b. Test Mode 4.

Test mode 4 was adopted as a final test of the enhanced susceptibility of the internal contacts. The current terminals were shifted one contact to the right (relative to mode 2), contacts 1 and 4 becoming the terminal contacts; contacts 2 and 3, the internal contacts. By so doing, a small (positive) end contact (contact 1) was substituted for the oversized end contact (contact L) used in mode 2.

The failure site inventory is shown in Table VII, which gives the sample size and the number of units failing at each contact. All six units were Al metallized, and all had low contact resistances (0.3 ohm). The predominant failure site was contact 2, all units experiencing failure at this site, whereas only three failures occurred at (the smaller, but external) contact 1. There was only one failure at contact 3, the other internal contact. Contacts 2 and 3 are the same size, i.e., 1.5 μm x 2.0 μm. However, the polycide line width under contact 3 is 3.0 μm whereas that under contact 2 is only 2.5 μm.

TABLE VII

Failure-site inventory for mode-4 CRTV failures.

SAMPLE SIZE	TOTAL FAILURE SITES			
	CONTACT 1	CONTACT 2	CONTACT 3	CONTACT 4
6	3	6	1	1

The current-density decrease is as expected; however, the decrease in both parameters simultaneously is anomalous, implying a (highly unlikely) negative activation energy for the failure process.

The proposed explanation for this result invokes the temperature distribution along line segment 1-2, a speculative illustration of which is given for the 25°C-ambient and 200°C-ambient conditions in Fig. 22. The mean temperature for the 25°C-ambient curve as drawn is roughly 410°C, approximately 30°C higher than that for the 200°C-ambient curve. However the 200°C-ambient curve is more uniform due to the uniform heating component provided by the 200°C chuck. Consequently, the endpoints of the 200°C-ambient curve, i.e., contacts 1 and 2, are roughly 50°C hotter than those of the 25°C-ambient curve.

The elevated-ambient failures were visually less dramatic than those at 25°C ambient. Only two units had failure sites visible at 1000X magnification, both of these being at contact 1. In six of the failed units the polycide line (while much increased in resistance) was still continuous, permitting post-failure contact resistance measurements on contacts 1, 2, and 3. In five

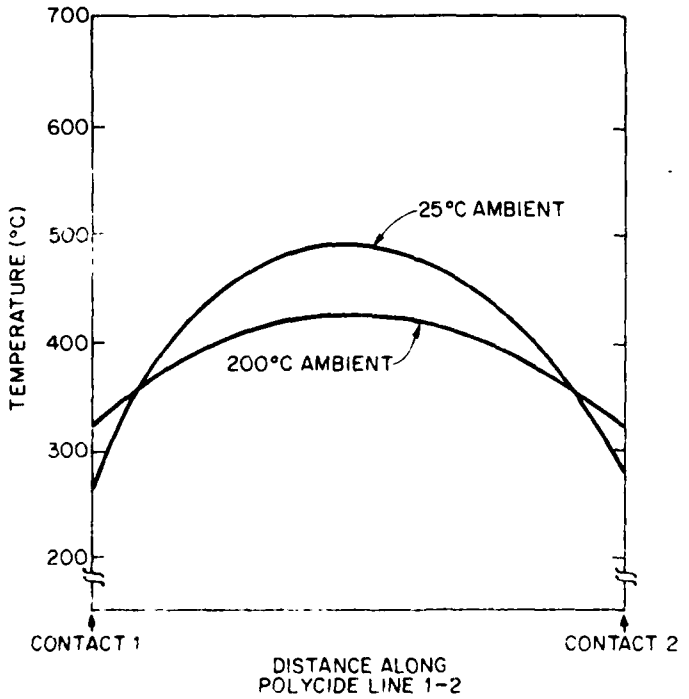
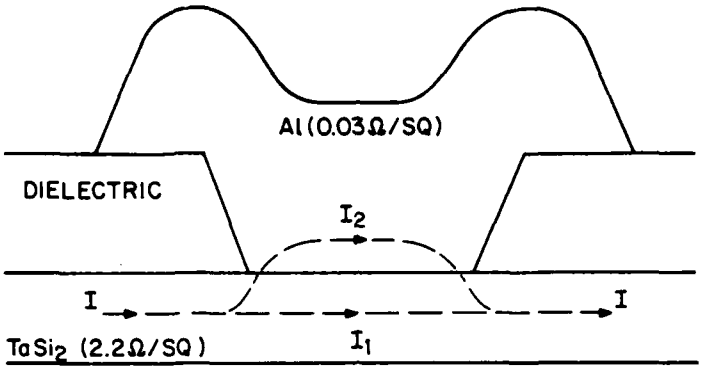


Figure 22. Speculative temperature distributions along line segment 1-2 during mode-2 powering at 25°C-ambient and 200°C-ambient temperatures.



$$I_1 + I_2 = I$$

$$I_2 \gg I_1 \text{ IF } R_C \approx 0$$

$$I_2 < I_1 \text{ IF } R_C \geq 1\Omega$$

Figure 21. Schematic cross-section diagram showing probable current paths for polycide-line current crossing an internal contact.

TABLE VI

Average current densities and temperatures at failure for Al-metallized CRTV units in mode-2 testing at 25°C, 100°C, and 200°C ambient temperatures.

AMBIENT TEMPERATURE (°C)	SAMPLE SIZE	AVERAGE VALUES AT FAILURE: CURRENT DENSITY (A/cm^2)	AVERAGE VALUES AT FAILURE: MEAN LINE TEMPERATURE (°C)
25	13	1.5×10^7	416
100	4	1.3×10^7	401
200	3	1.0×10^7	374

current density at failure and mean temperature of line segment 1-2 at failure, averaged over each group. It is seen that both current density and mean line temperature at failure decrease monotonically with increasing ambient temperatur

TABLE V

Failure-site inventory for mode-2 CRTV failures.

SAMPLE GROUP	SAMPLE SIZE	TOTAL FAILURE SITES			
		CONTACT L	CONTACT 1	CONTACT 2	CONTACT 3
AL-1%SI EARLY	7	0	0	0	7
AL-1%SI INTERMED.	3	1	0	1	3
AL-1%SI MAINSTREAM	8	3	6	2	4
AL MAINSTREAM	13	2	13	1	4

shows a cross section of the contact cut along the length of the polyside line. The Al plug (interconnect) is a very effective shunt if the contact resistance R_C is insignificant, in which case I_2, the current passing in and out through the contact, is much greater than I_1, the current flowing in the $TaSi_2$ line under the contact. However for high values of R_C, I_2 becomes insignificant, and virtually no current passes through the contact.

Murarka et. al. [8] report that Rutherford backscattering (RBS) measurements detected no $TaSi_2$/Al interaction for temperature/time products ranging up to 550°C/60 minutes. However, the CRTV line failures at internal contacts strongly suggest that such interaction is occurring during powering, and that it is damaging the $TaSi_2$ film under the contact throughout its depth. If this were not the case, i.e., if damage was being done at the contact interface only, the current component I_2 would drop as R_C increased, and the damage process would be self-limiting, precluding the catastrophic failures observed at the internal contacts.

Seven units were subjected to mode-2 tests on a heated chuck. All of these units were Al-metallized; four were run at 100°C ambient; three at 200°C ambient. As in the case of the room-ambient (Al-metallized) units, the failure distributions were narrow. The results are listed in Table VI, which gives the

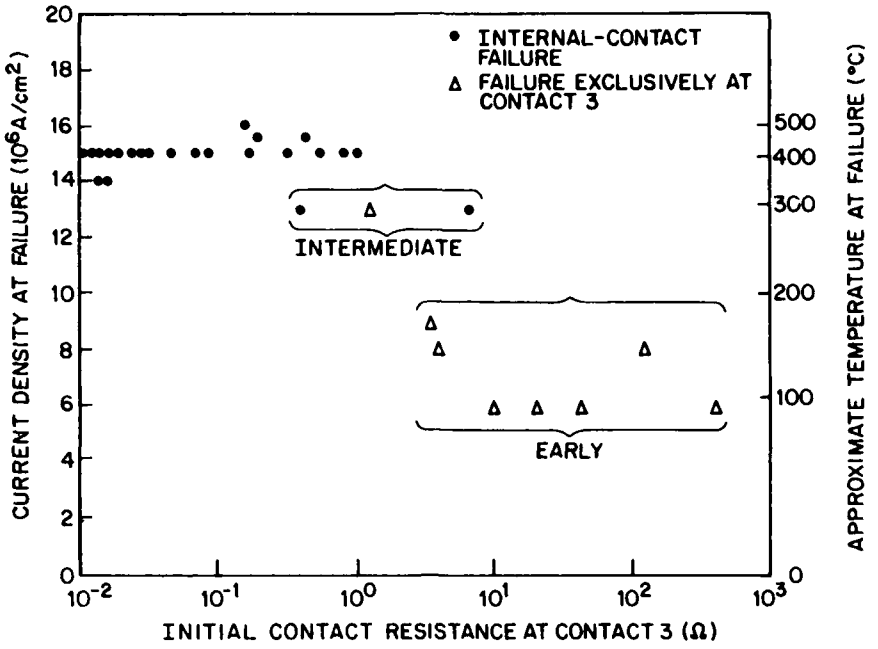


Figure 20. Current density at failure (and approximate temperature at failure) versus initial contact resistance at contact 3 for early, intermediate, and mainstream mode-2 failures.

The distribution of failure sites is given in Table V, in which column 1 lists the four sample groups, as defined previously; column 2 lists the number of units in each group; and columns 3 through 6 list the total number of failure sites associated with each contact.

Contact 1 is by far the predominant failure site in the two mainstream groups, particularly in the Al-metallized group where all of the chips had a failure site at this contact. There are three probable reasons why contact 1 was the weak link in these groups: (1) its internal location in the Joule-heated line rendered it hotter than the end contacts, (2) it is smaller than contact 2, the other internal contact, and (3) when its contact resistance to Al or Al-Si is significantly less than 1 ohm it serves as an active contact, passing current into the (0.03 ohm per square) Al shorting "plug" at the left side of the contact interface and drawing current back into the $TaSi_2$ at the right side.

Conversely, the internal contacts in the early-failure group were spared because their high contact resistance substantially reduced current flow to the Al shorting plug. The situation is illustrated in Fig. 21, which

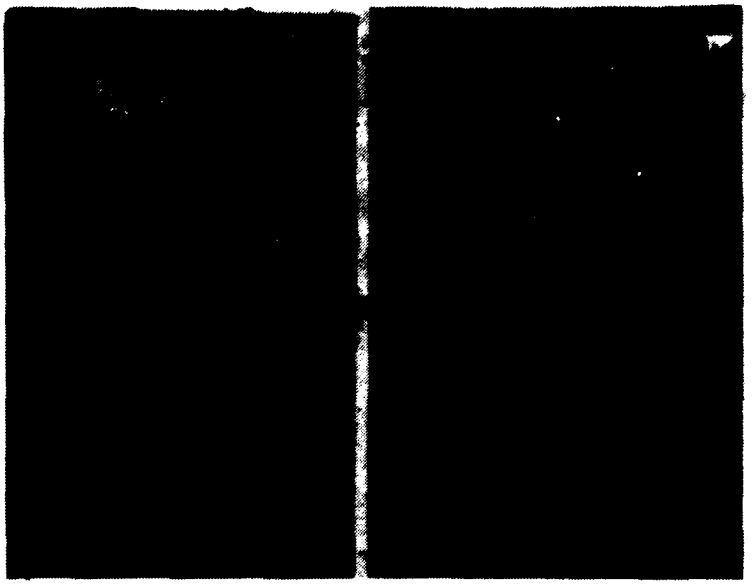


Figure 18. Photomicrograph of failure site in Al-1%Si metallized, mode-2 early failure: contact 3 and vicinity at 1000X magnification, showing open polycide line.

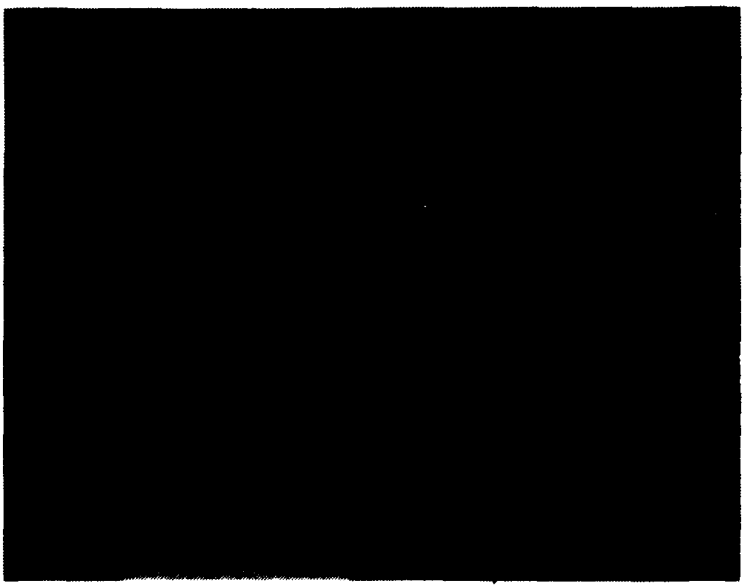


Figure 19. Photomicrograph of failure site in Al-1%Si metallized, mode-2 early failure: contact 3 and vicinity at 1000X magnification, showing open Al-Si line.

Figure 30. Photomicrograph of failure site in Al-metallized mode-7 failure showing melting along polycide line and at contact C: contact C and vicinity at 500X magnification.

which appears to be isolated, and in which gross melting has occurred. However, the polycide line segment extending from this failure site to contact C appears to have a narrow "streamer" above it which has the appearance of Al. Also, the Al above contact C has experienced gross melting. These observations suggest migration of Al along the polycide line, as had been reported previously by Lloyd et. al. [27].

e. Contact Strings.

The visual suggestions of Al migration along the polycide line in Fig. 30 are supported by some of the results of electrical measurements made during high-current testing of the contact strings. The tests performed were 10-minute-increment tests to failure; the measurements were in-situ measurements of terminal voltage at one-minute increments, and measurements of terminal voltage at 1mA between all 10-minute powering increments.

An example of the results is shown in Fig. 31, in which terminal resistance (as calculated from the terminal voltage) is plotted versus current. Two sets of points are shown; those measured in-situ at the 10-minute mark at each powering current, and those measured at 1mA immediately after the corresponding

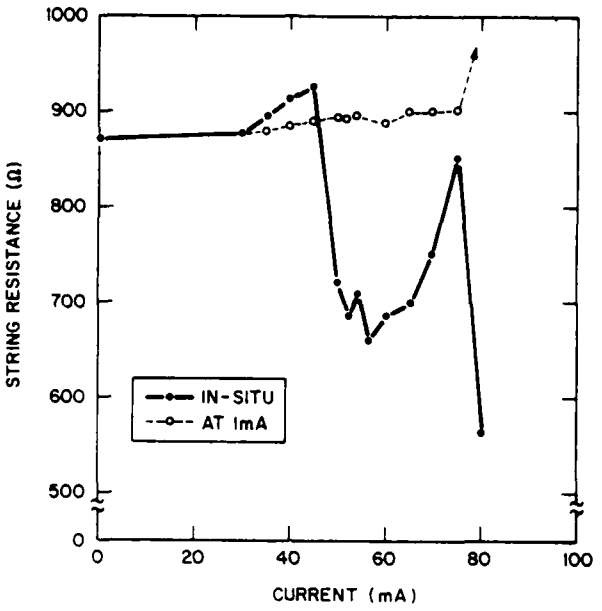


Figure 31. Series-string terminal resistance versus current: in-situ measurements, and measurements at 1mA after 10-minute powering increments at each current.

in-situ measurement and current reduction. The readings at 1mA are well behaved right up to failure at 80mA, rising gradually from the initial value of 870 ohms to 900 ohms after 75mA. This (~3 percent) increase in resistance is the result of an overall temperature increase in the chip and mounting chuck (ambient) which occurs during powering, and amounts to about 10°C after 10 minutes at 75mA.

In contrast, the in-situ results in Fig. 31 are highly anomalous and (above 45mA) erratic. Instead of increasing parabolically with current, as had the polycide line resistances in Figs. 10 and 25, the string resistance increased very little below 45mA, and dropped precipitously above 45mA.

One possible explanation is Al migration along the polycide line segments. The string geometry favors this, with short polycide segments alternating with Al segments, each of the latter representing a potential migration source. However, such an explanation does not account for the constancy of the 1mA curve in Fig. 31, unless the migrated Al somehow becomes electrically disconnected from the polycide line (delaminated?) when the current is lowered.

3. Material Analyses

The material analysis techniques employed in this program were scanning electron microscopy (SEM), electron probe microanalysis (EPM), and Auger electron spectroscopy (AES).

Other techniques considered include secondary ion mass spectroscopy (SIMS) and transmission electron microscopy (TEM); however, technique/sample compatibility problems precluded the use of either; SIMS requiring a much larger sampling area than provided by any of the CRTV features, and TEM having difficulties in sample preparation and feature targeting (during sample thinning).

Several of the questions and possibilites implied by the high-current-testing results were investigated, including Ta loss or buildup along damaged polycide line segments, Ta loss or buildup at contact sites, Al migration into $TaSi_2$, and Ta migration into Al.

The question of Ta loss during polycide-line damage was addressed by taking EPM scans along the lengths of several damaged polycide lines. Results for one such scan are shown in Fig. 32, in which the Ta ($L\alpha$) x-ray signal from the polycide line is plotted versus distance along the polycide line. Zero on the distance scale represents the center of contact 1. The region of visible damage in this chip (a mode-2 mainstream failure) extended out from contact 1 to a distance of approximately 80 μm. The Ta signal in this region is seen to vary up and down precipitously, levelling off only when the undamaged region is reached. Typical of all such traces, Fig. 32 indicates a net loss of Ta in the damaged area.

However, the highest amplitude Ta signal in Fig. 32 is at the contact site, underneath the Al film. This suggested that some of the missing Ta may have migrated to the contacts. SEM photos of several contact areas, taken after the Al film had been stripped away (in a hot phosphoric-acid etch), tended to support such a hypothesis.

Four such photos are presented in Figs. 33, 34, 35 and 36, which show contacts 1, 2, 3, and 4, respectively, of a chip which had experienced mainstream failure in mode 2, and in which the visible failure site (under optical-microscope inspection) had extended from approximately 80 μm to the left of contact 1 to approximately 10 μm to the right of contact 1.

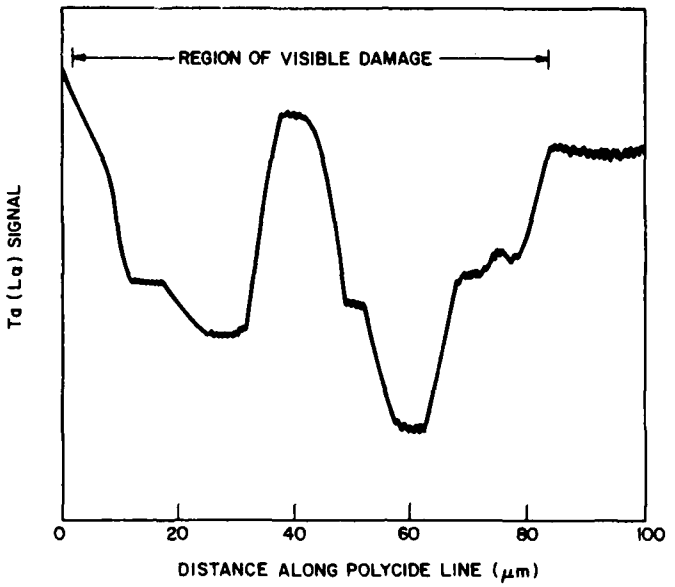


Figure 32. Ta (Lα) EPM x-ray counts versus distance along polycide line of failed CRTV unit.

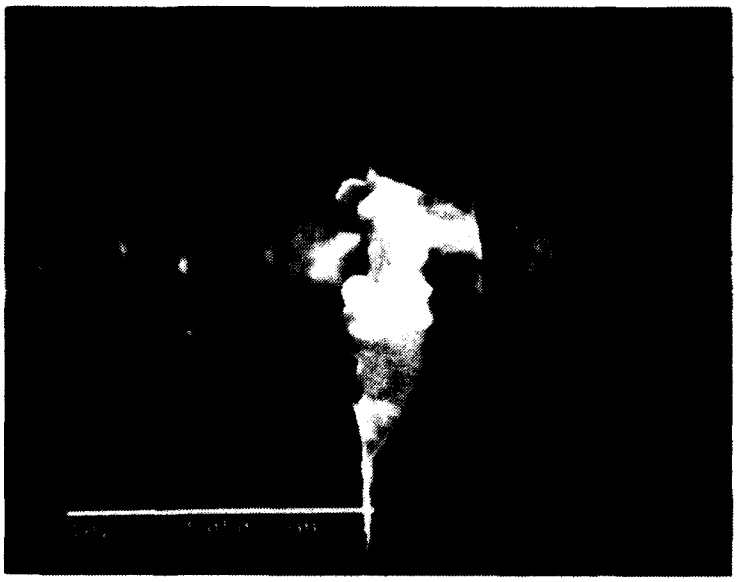


Figure 33. Scanning-electron micrograph of CRTV mode-2 mainstream failure at contact 1, in which Al film had been stripped: contact 1 and vicinity at 5000X magnification.

Figure 33, taken at 5000X magnification, shows the damaged polycide line extending to the left, a large (overexposed) protrusion at the contact site,

and a residue along the site of the stripped Al line. Neither the protrusion nor the residue was affected by doubling the Al stripping time in the phosphoric-acid etchant.

Figures 34 to 36 were all taken at a nominal 10,000X magnification; Fig. 36, on the unpowered contact 4, serving as a standard. In Fig. 35, contact 3 and vicinity show both protrusion and residue, while contact 2 in Fig. 34 shows only a (relatively small) protrusion. The protrusions at contacts 2 and 3, neither of which were visible failure sites, provide further evidence of pre-failure degradation of contacts in mainstream units.

Both AES surface analysis and EPM counts were run on samples with similar histories in an attempt to determine the type and amount of material(s) comprising the protrusion and residue. The AES samples were stripped of Al and elemental surface scans were made. No Ta was detected in the residue of the Al line. However, Cl, S, and C were all detected both in the residue and in the protrusion. Elemental scans repeated after several hundred Angstroms of sputter etching yielded the same elements, all of which are constituent elements of the reagents and/or plasmas used in wafer processing. However, there was still no Ta observed in the residue. EPM experiments likewise were unable to detect any signs of Ta migration along powered Al (or Al-Si) lines, either in failed units or in heavily-powered but unfailed units.

EPM experiments were also performed to determine the relative amounts of Ta (numbers of Ta atoms) in the powered contacts as compared with those in unpowered contacts. The measurement was performed by targeting the 25 KeV electron beam on the center of the contact being measured, taking a 30-second Ta ($L\alpha$) count, moving the beam to an undamaged position on the adjacent polycide line (having the same linewidth as that at the contact site), taking a second 30-second count, and dividing the second count into the first count. The resulting counts ratio provided an approximation of the ratio of the number of Ta atoms under the contact to that at an undamaged line site of the same width. By comparing the ratios obtained for powered and unpowered contacts, information concerning Ta migration to contact sites was obtained.

The results are shown in Table VIII, in which three samples powered to failure in mode 2 are represented, an Al-metallized mainstream failure (420°C, at contact 1), an Al-1%Si metallized mainstream failure (450°C, at contact 1), and an Al-1%Si metallized early failure (90°C, at contact 3). Below the sample descriptions, the bottom seven rows in Table VIII give the counts ratios

Figure 34. Scanning-electron micrograph of the same CRTV unit shown in Figure 33: contact 2 and vicinity at 10,000X magnification.

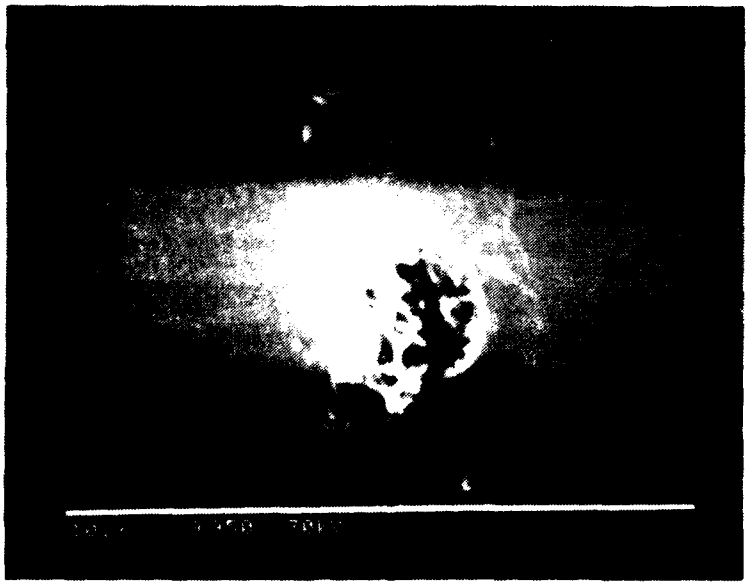


Figure 35. Scanning-electron micrograph of the same CRTV unit shown in Figure 33: contact 3 and vicinity at 10,000X magnification.

Figure 36. Scanning-electron micrograph of the same CRTV unit shown in Figure 33, contact 4 and vicinity at 10,000X magnification.

measured for each sample for contacts 1 to 7. All of the ratios for unpowered contacts (contacts 4 to 7) are below 1, the reason being that the Ta (Lα) signal from the contacts had to pass through 12 kÅ of (unstripped) Al or Al-1%Si, whereas the signal from the line had only to pass through the 4 kÅ interlevel dielectric. Among the powered contacts, none of those on the unit experiencing early failure had significantly higher count ratios than the unpowered contacts. However, in both mainstream failures the count ratio at the failed contact, i.e., contact 1, was unusually high (~1.0). In addition, the ratio at contact 3 was high in the Al-1%Si metallized mainstream unit.

These results suggest significant Ta migration to contact 1 in both mainstream failures, and also to contact 3 in the Al-1%Si metallized failure, but no significant Ta migration in the early failure. They are entirely consistent with the results of microscope examinations of mode-2 failure sites (Figs. 13 to 16, 18 and 19, and Table V), in which the mainstream failures involve extended segments of the polycide line, whereas early failures are highly localized at contacts, and in which contact 1 predominates strongly over contact 3 as a mainstream failure site in Al metallized units, but not in Al-1%Si metallized units.

The highly localized nature of early failures (shown previously in Figs. 18 and 19) is illustrated further in Fig. 37, which shows a 10,000X SEM photograph of a mode 6 (+) early failure at contact 2. Failure is seen to occur in the (vertically running) polycide line immediately above the Al-Si stripe where

TABLE VIII

Ta (Lα) x-ray count ratios for CRTV contacts 1 to 7 on three units tested to failure in mode 2.

METALLIZATION	Al	Al-1%Si	Al-1%Si
FAILURE SITE	1	1	3
TEMPERATURE AT FAILURE (°C)	420	450	90
1	1.02	1.01	0.82
2	0.85	0.82	0.87
3	0.72	1.03	0.62
4	0.82	0.86	0.93
5	0.79	0.86	0.84
6	0.75	0.73	0.82
7	0.69	0.91	0.78

a "blowout" appears with local delamination. However, the polycide-line damage appears to extend less than 2 micrometers above the edge of the Al-Si stripe.

EPM was also used to investigate the possibility of Al migration along the polycide line. A total of six units were tested, two each of mode-2 early failures, mode-2 mainstream failures, and mode-7 (-) failures. The metal interconnect was stripped in hot phosphoric acid from all four mode-2 units before analysis to prevent the signal from any unetchable Al in the contact areas from being overwhelmed by this interconnect signal.

Results for the four mode-2 units are shown in Fig. 38, in which the (30-second) Al (Kα) count is plotted on a logarithmic scale versus distance along the polycide line, and where the distance abscissa is labelled by contact number (or letter). The length of the powered line segment is indicated at the

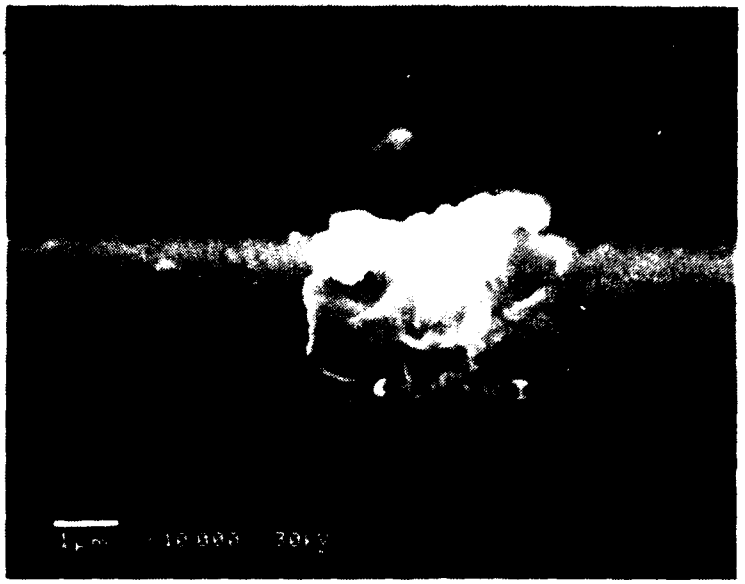


Figure 37. Scanning-electron micrograph of CRTV mode-2 early failure from which Al-1%Si film has not been stripped: contact 3 and vicinity at 10,000X magnification.

top of the figure. Counts were taken beyond the powered segment, i.e., at contact 4 and 40 μm to the left of contact 4, to determine a background noise level. This noise level was found to be roughly 100 counts. Accordingly, all counts below 100 were ignored and not plotted.

The results in Fig. 38 are clear-cut and consistent, showing Al migration along the powered line segment in both mainstream failures, the absence of such migration in the early failures, and a large signal of unetchable Al at the (contact-3) early-failure site. The Al appearing along the powered line in the standard failures is not necessarily unetchable; it was protected by the interlevel dielectric during the Al etching step.

A standard for the Al signal was generated by measuring Al (Kα) counts at contact sites of several unstripped units. The average number of counts from the 12kÅ Al film on such units was approximately 50,000. Thus, the two early-failure counts in Fig. 38 (6300 and 1050) represent equivalent thicknesses of roughly 1kÅ and 0.2kÅ of unetchable Al, respectively. It was not determined whether this Al had reacted with the Ta to form a compound. However, the existence of two such compounds has been reported [41], and such determination represents a potential area for future investigation.

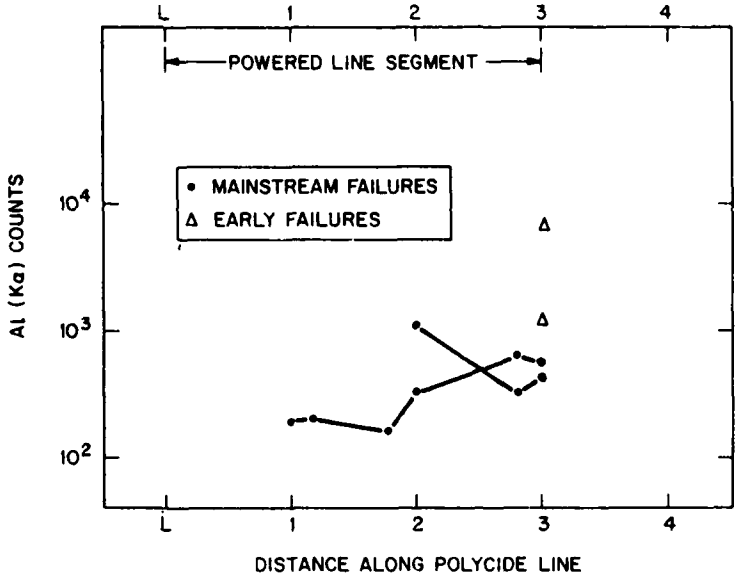


Figure 38. Al (Kα) EPM x-ray counts versus distance along polycide line for CRTV mode-2 mainstream failures and early failures in which the Al (or Al-Si) film had been stripped.

The two additional mode-7 failures in this Al migration experiment are the same units shown in Figs. 29 and 30. EPM results are shown in Fig. 39 where Al (Kα) counts are plotted versus distance along the polycide line segment between contact 4 and contact C (contact 4 being at zero; contact C, at 250 μm). Boundaries of the regions of visible failure are indicated on each curve by vertical bars, counts being taken to the left of, to the right of, and within these boundaries. The visual observation of an Al stringer in Fig. 30 is confirmed by the very high count (10,000) in the upper curve of Fig. 39 at 210 μm, a point to the right of the region of gross visual damage. The peak count inside the damaged area is 27,000, within a factor of 2 of that obtained at the contacts. (The Al was not stripped from these two units for fear of stripping Al from the damaged area, over which the interlevel dielectric had clearly been shattered.)

The unit represented by the lower curve in Fig. 39 was the one in which the visual damage appeared to be isolated along the line with no contact involvement (Fig. 29). However, this curve shows significant Al signals both within and beyond the visible damaged regions, proving that there was, in fact, contact involvement in the failure. Thus, all CRTV line failures, and all

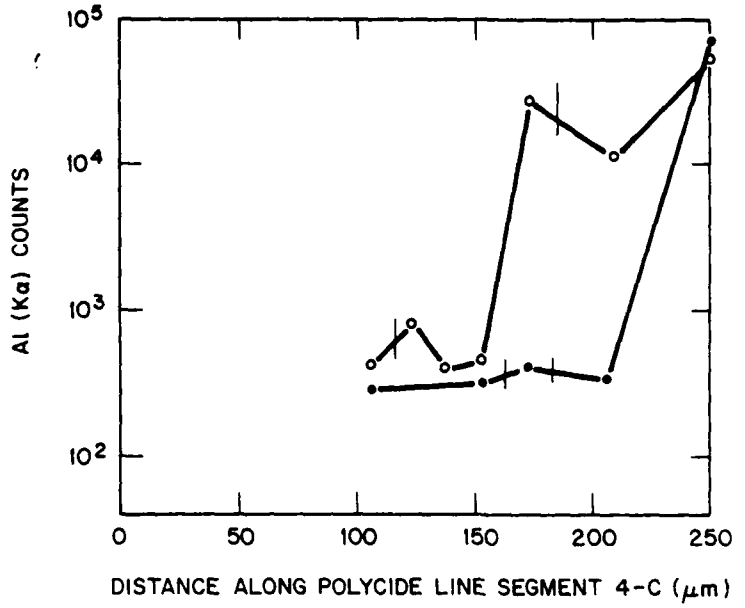


Figure 39. Al (Kα) EPM x-ray counts versus distance along polycide line for the CRTV mode-7 failures pictured in Figures 29 and 30.

individual failure sites observed in this program, have been shown to be associated with a $TaSi_2$/Al (Al-Si) contact.

The principal reliability concern uncovered in this program is represented by the early failures associated directly with, and physically isolated at, contact sites. As shown in Figs. 20 and 24, these failures can occur within minutes at polycide-line current densities as low as 5×10^6 A/cm^2 (or currents as low as 25mA, which corresponds to a current density of less than 10^6 A/cm^2 when calculated based on the nominal interface area of the contact). The one redeeming feature of this failure mode is that it can be prevented by proper processing, or by detection and rejection of susceptible wafers and chips using contact resistance measurements.

The mainstream failures represent a less-severe reliability concern because of the higher levels of stress required for failure, the remarkably narrow distribution of these levels, and the relatively minor degradation in electrical parameters until just prior to failure. However, they also represent a concern which is more basic, because the evident causes, i.e., Al diffusion across and migration along the polycide line, and Ta migration toward contacts, occur even in properly-processed devices.

The results indicate that Al migrates in from the positive contact, moving from the positive end of the polycide line segment toward the negative end. Migration in this direction is opposite that expected on the basis of momentum transfer from electrons to Al atoms. In at least one instance (Fig. 30) the Al migration had occurred along the $TaSi_2$/interlevel-dielectric interface.

Our EPM results did not distinguish which interface the Al was migrating along in the other units. However, Lloyd et. al. [27] had previously reported Al migration along the $TaSi_2$/polysilicon interface. This would imply that Al had diffused through the $TaSi_2$ film at the contact site, an occurrence which was implied (but not proven) by the predominance of internal-contact failures in mode 2.

The results thus uncover many questions concerning the specific mechanisms leading to mainstream failure, and of their onset thresholds, development sequences, and activation energies. Specific recommendations for future efforts along these lines are presented in Section V-B. The general approach recommended would start with the establishment of an improved understanding of these mechanisms through use of test-vehicle layouts which address the special needs of polycide electromigration testing as uncovered in the present investigation, and through more detailed and sensitive analyses of failures and of heavily powered units. Effort would then turn to investigations of these (now better understood) mechanisms at progressively lower stressing levels and earlier stages in their development.

V. CONCLUSIONS AND RECOMMENDATIONS

CONCLUSIONS

Conclusions are presented separately for different accelerated-testing tegories: (1) thermal testing under static-bias or unbiased conditions d (2) high-current testing. The first category includes both temperature- cle and step-stress bias-life tests on the high-speed QMOS logic circuits d thermal-shock tests on the CRTV parametric test circuits. The second tegory constitutes the high-current tests on the CRTV circuits.

Thermal Testing.

It is concluded from the results of temperature-cycling and step-stress sts on QMOS circuits, and from thermal shock tests on CRTV circuits, that lycide line integrity, underlying gate dielectric integrity, and circuit nction, including such important parametric measures as n-channel transistor reshold, p-channel transistor threshold, and propagation delays, are not graded by such accelerated reliability tests.

All 50 polycide-gate QMOS units survived 1000 cycles of thermal cycling -65°C to +150°C) with performance levels comparable to, or better than, the 50 olysilicon-gate control units. In step-stress bias life tests (125°C to 50°C), one polycide-gate unit out of 27 experienced parametric failure, ompared with three failures among the 27 control units. The single polycide- nit failure was traced to an in-process scratch which thinned the gate oxide, nereby increasing its leakage current after the 250°C increment of bias-life esting.

No significant changes in polycide line resistance were observed after 30 ycles of thermal shock (-70°C to +100°C) on CRTV units, and shocked units in ubsequent high-current testing had failure levels comparable to those obtained n corresponding unshocked units. Shocked and unshocked test and control units ad similar failure distributions in capacitor breakdown tests.

High-Current Testing.

The principal conclusions from the high-current-test results are (1) that ne predominant weak link in the polycide/Al (or Al-1%Si) multilevel-conductor tructure is the $TaSi_2$/Al (or Al-1%Si) interlevel contact, and (2) that an nitial interlevel contact resistance, which is only moderately high ($\gtrsim$ 1 ohm),

presents a significant threat to the reliability of circuits which draw
bstantial interlevel currents.

Mean polycide-line temperature and current density at catastrophic failure
der 10-minute-increment powering correlated well with initial contact resis-
nce. Early failures were consistently observed for units with initial con-
ct resistance greater than approximately 1 ohm, with temperatures at failure
nging downward from approximately 200°C to less than 100°C, and current den-
ties ranging downward from approximately 1.0×10^7 A/cm^2 to 5×10^6 A/cm^2
th increasing initial contact resistance. Units with initial contact resis-
nces less than 1 ohm (mainstream failures) were characterized by narrow
ilure distributions at substantially higher temperatures (360°C to 500°C)
d current densities (1.4×10^7 A/cm^2 to 1.8×10^7 A/cm^2).

Early failures and mainstream failures displayed contrasting failure site
nfigurations, early failures being highly localized at contacts where runaway
ule heating had evidently occurred, while mainstream failure sites extended
om contacts along the polycide line for distances up to several hundred
crometers. However, mainstream failures were ultimately also traced to the
ntacts through two consistent observations: (1) the presence of Al, which
d migrated from the contact areas, along (and sometimes beyond) the failed
rtions of the polycide line, and (2) the absence of polycide-line failure
tes fully isolated from contacts. A Ta buildup in contact areas was observed
mainstream failures but not in early failures, consistent with their respec-
ive extended and highly localized regions of polycide damage.

Polarity effects were consistent but complex, early failures occurring at
e negatively-biased contact; mainstream failures at the positively-biased
ntact. However, in the mainstream failures, pre-failure degradation in
ntact resistance was observed at the negative contact as well as the positive
ntact, and indications of Ta buildup at both contacts were observed after
it failure. The results indicate that Al along the polycide line had entered
the positive contact and migrated along the direction of current flow, i.e.,
posite to the direction of the force experienced through momentum transfer
om electrons. However, the negative contact was not eliminated as an Al
urce, and Al migration from both contacts along polycide-line temperature
radients is a possibility.

All $TaSi_2$/Al initial contact resistances were well below 1 ohm, consequently all of the early failures were on Al-1%Si metallized units. Stripping the metal from these early failures revealed dense silicon-precipitate films (freckles) on the interlevel dielectric surface. It is concluded by inference that such freckles in contact areas inhibited the formation of consistently good contacts, and were therefore likely contributors to the early failures.

Pre-failure electrical degradation in mainstream failures was limited to contact areas, line resistances remaining stable. While modest increases in contact resistances ($\lesssim$ 3 ohms) were observed during in-situ measurements, these were not interpreted as failures in this investigation since their extent was insufficient to have significant impact on circuit performance. However, the observations of Al along unfailed sections of polycide line, and of extra Ta in powered, but unfailed contacts suggest the presence of pre-failure mechanical degradation, which would be an important topic for future investigations.

B. RECOMMENDATIONS

1. Design, Processing and Testing.

All of the recommendations arising from this investigation focus on the interlevel contact, the weak link in the polycide/metal multilevel structure. Consequently, the obvious recommendation concerning design of such circuits' physical layouts is to provide the maximum practical interface area at all contacts drawing substantial interlevel currents. This can be accomplished either by using a "dogbone" contact structure or by using multiple (redundant) contacts.

Recommendations for maximum powering conditions are made with reference to the limitations of the high-current experiments, as outlined in section IV-B2C, and with the assumption that early failures are eliminated. Within this context, the activation energy for mainstream failure was calculated (very roughly) to be 1.3 eV. Combined with measured failure times of a few hours at 340°C (at 1.5 x 10^7 A/cm^2), an Arrhenius calculation yields failure times of roughly 10,000h at 200°C and > 10^6h at 125°C (at 1.5 x 10^7 A/cm^2). These latter two conditions are fictitious, a lower current density, i.e., 1.0 x 10^7 A/cm^2, resulting in a mean line temperature of 200°C at room ambient (see Fig. 10).

It is our judgment that this 1 x 10^7 A/cm^2 value would represent a reasonable upper limit for room-ambient operation. However, for elevated ambients it is felt that the upper limit should be lowered (according to Fig. 10) to maintain mean line temperature below 200°C. This would result, for example, in an upper limit of 6 x 10^6 A/cm^2 for operation in a 100°C ambient.

Processing recommendations include thorough cleaning of contacts prior to metal-interconnect film deposition, either performing the cleaning process in situ or minimizing the time between cleaning and deposition-system pumpdown, and proper maintenance and operation of the metal deposition system. Such practices will minimize the probability of high-resistance contacts. However, when the metal is an Al-Si alloy, silicon precipitation on contact interfaces is always a possibility. This possibility, together with the relatively low values of contact resistance at which contacts become less reliable, necessitates thorough and specific testing at the wafer level, and preferably also at the circuit level.

The recommended wafer- and circuit-level tests are contact resistance measurements on structures similar to the CRTV. Contact resistance tests are often performed on contact strings or lengths of conductor terminated at either end by a contact. In either case contact resistance is calculated by subtracting the (often calculated rather than independently measured) line resistance from the terminal resistance. It is emphasized that such methods are inadequate for this situation because the (~ 1 ohm) threshold for decreased reliability corresponds to only ~ 0.4 square of the conductor material. Only measurements which isolate and measure contacts individually (such as those illustrated in Fig. 8 and 23) have the sensitivity required by this situation.

It is recommended that a minimum of 25 individual contact resistance measurements be made on each wafer in the wafer-acceptance tests, and that, whenever possible, CRTV-type structures be included on individual-circuit patterns, to be measured during the circuit-probing operation.

2. *Future Investigations.*

Areas for future investigations suggested by the results of this program include a closer examination into the mechanisms leading to mainstream failures. The objective of such an investigation would be to better understand the root causes of failure, to identify the material degradations which accompany (or

precede) the first signs of electrical degradation, and to define their thresholds.

Unanswered questions involve the possibility of Al diffusion through the $TaSi_2$ film, the dynamics of Al migration along the $TaSi_2$/interlevel-dielectric interface and along the $TaSi_2$/polysilicon interface, the direction(s) of such migrations, the dynamics and directions of Ta and Si migrations, and solid-state reactions involving Ta, Si, and Al. Another complicating factor of potential significance is the effect of residues from processing on such mechanisms.

The suggested approach to such investigations is similar to that of the present program, combining electrical testing with material analytical techniques. Suggested refinements on the approach include greater concentration on material analysis, closer integration of electrical testing with material analysis, and the design and utilization of an improved test vehicle layout.

Layout improvements suggested by the CRTV results include the incorporation of voltage taps for line-resistance measurements on the polycide mask level rather than the metal level to avoid the complicating effects of internal $TaSi_2$/Al contacts, and the incorporation of polycide line segments with a multiplicity of close-spaced voltage taps to permit detailed measurements of line-temperature distribution, particularly near contacts.

Closer integration of material analysis and electrical testing could be accomplished by in-situ analysis during powering of (wire-bonded) units. Non-destructive test methods such as SEM and EPM would be particularly valuable for such in-situ analyses.

The dominant role played by migrations to and from the $TaSi_2$/Al (or Al-Si) interface in the mainstream failures suggest both the opportunity and ultimate necessity for testing of $TaSi_2$/metal interlevel structures in which the metal is a barrier/Al composite. Such composites are increasingly strong candidates for metallization levels which make contact to silicon in shallow junction devices. For circuits in which such levels also make contact to a polycide underlayer, a barrier metal could enhance reliability if its barrier properties are maintained during powering. However, the potential for undermining reliability also exists, and would therefore have to be tested.

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